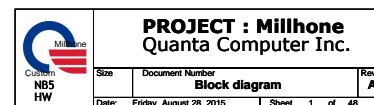
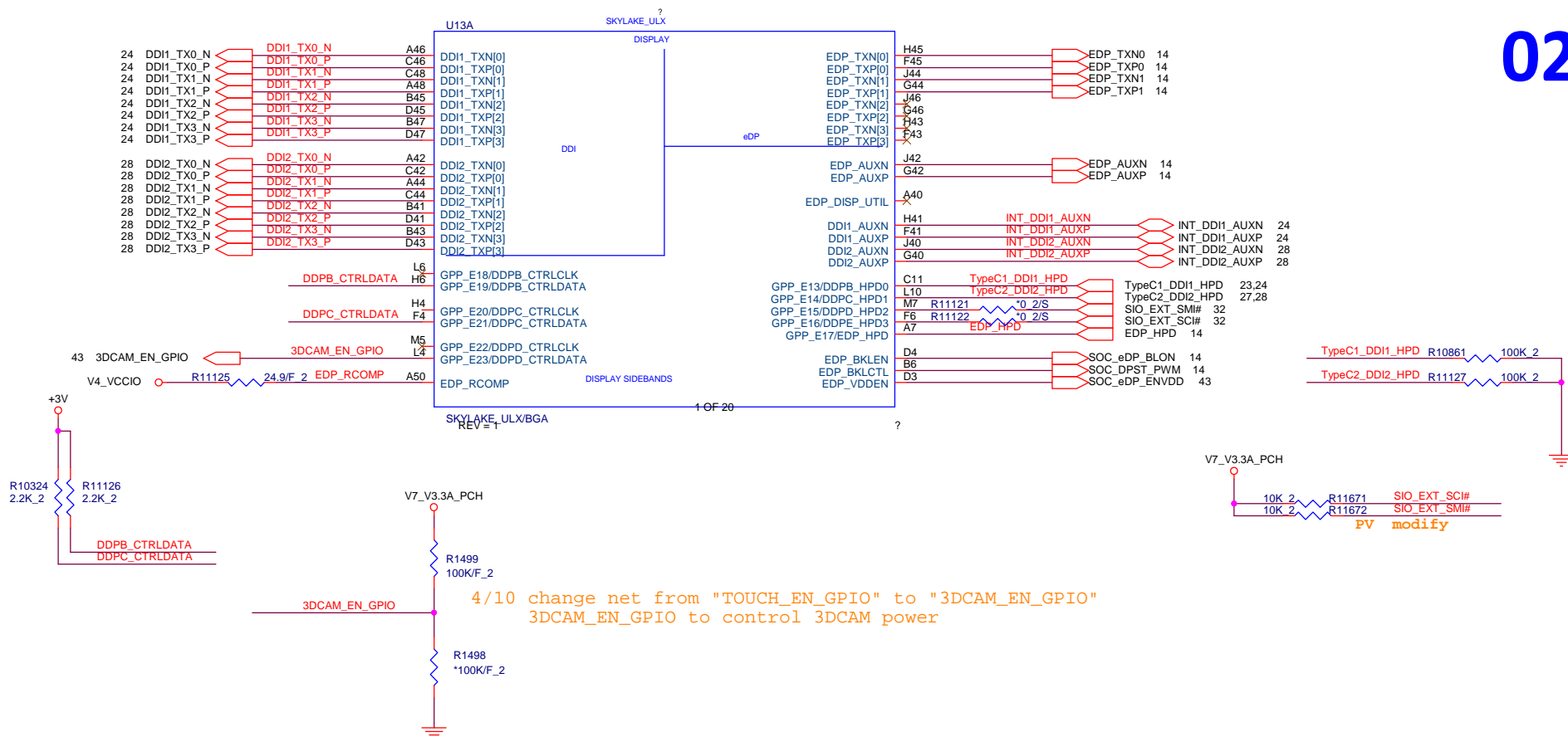


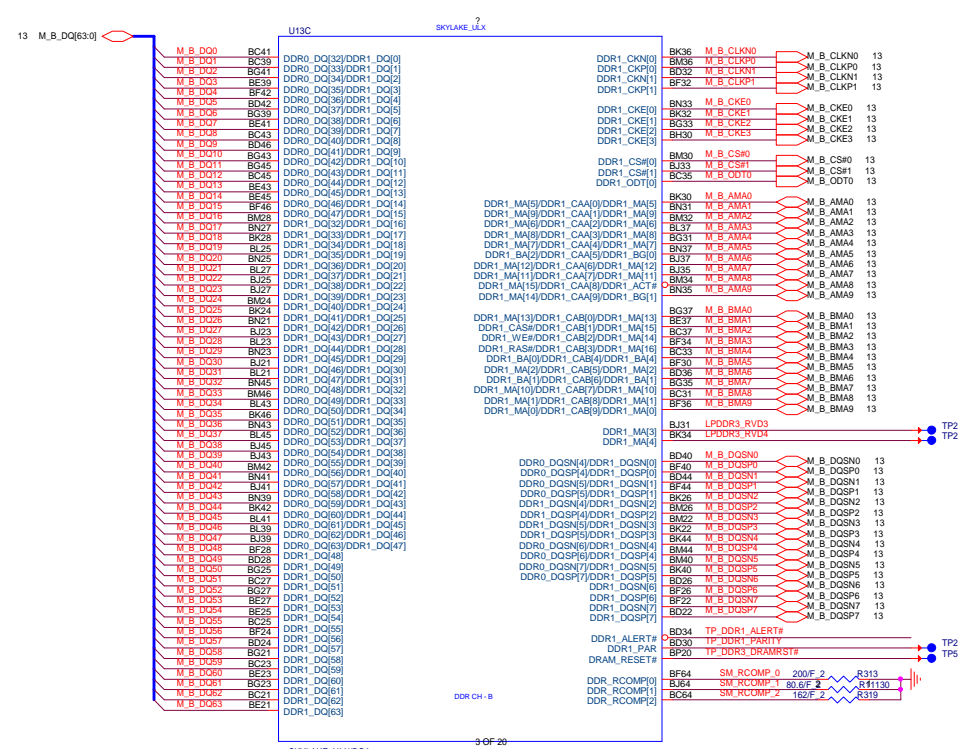
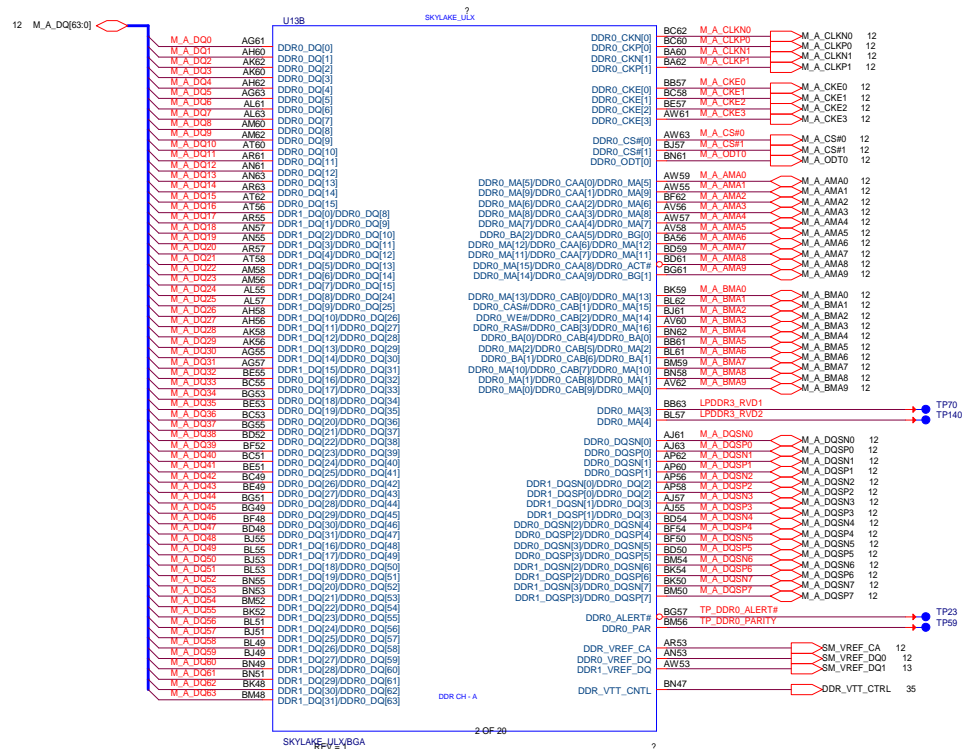
01

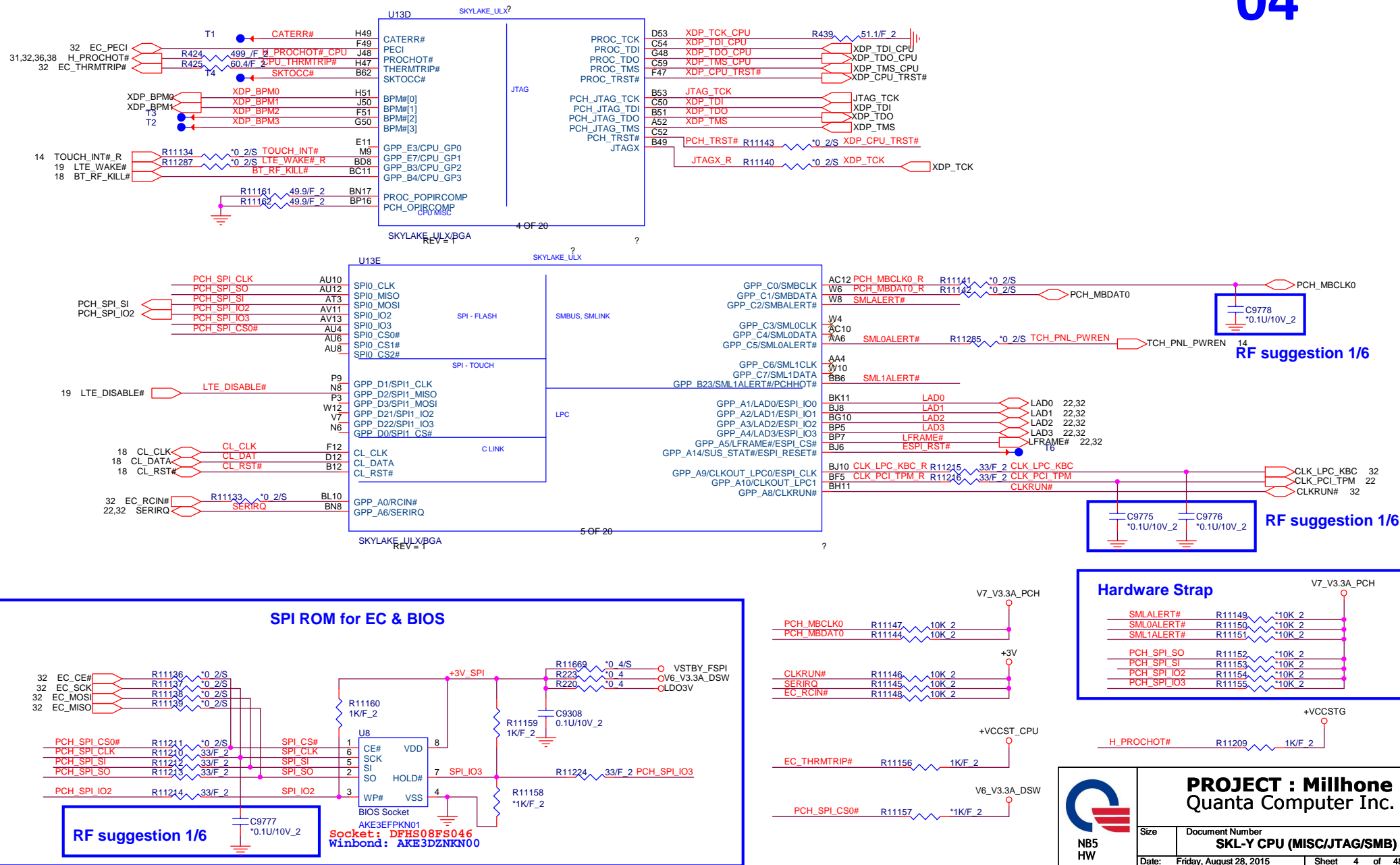


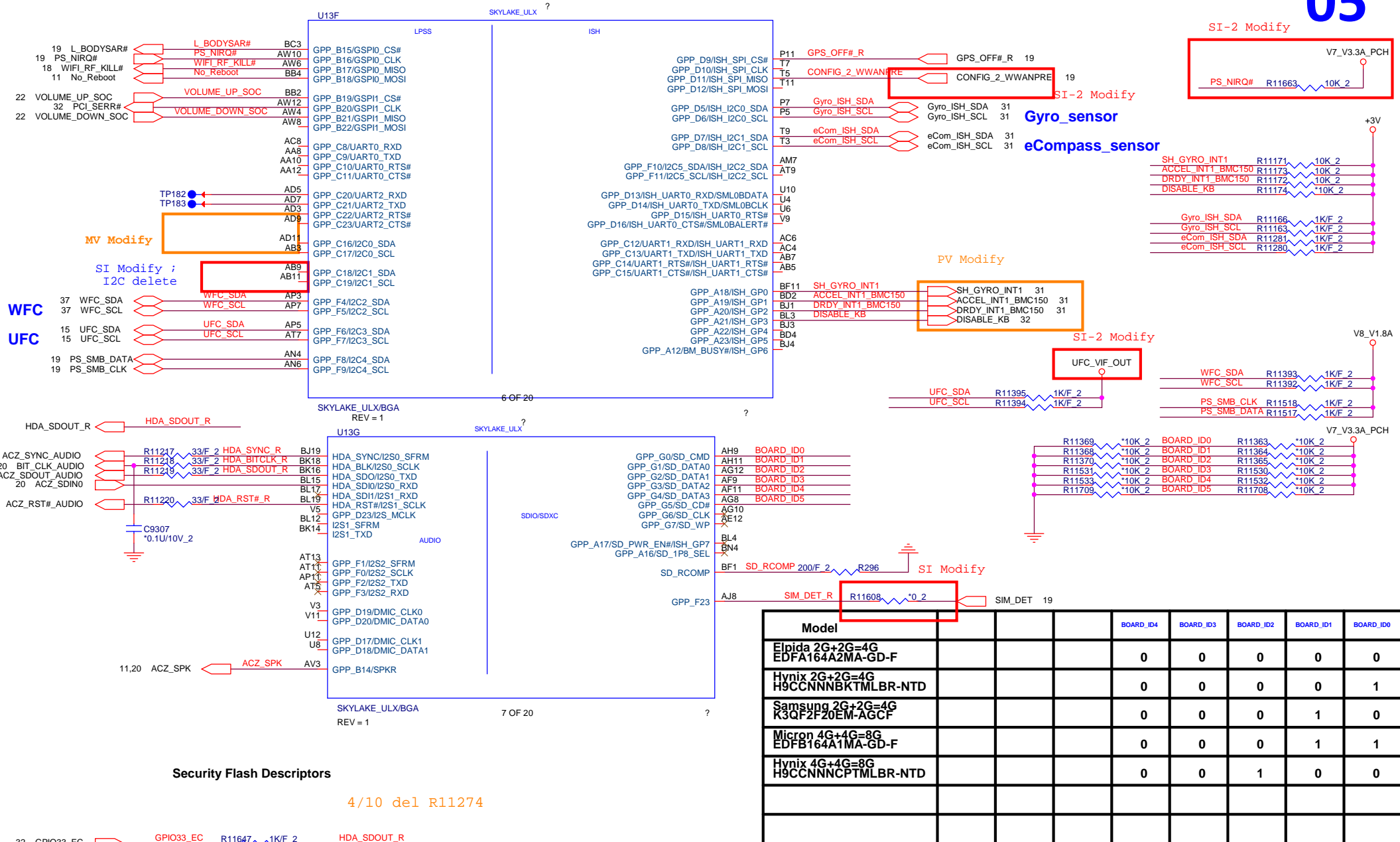


PROJECT : Millhone
Quanta Computer Inc.

Size	Document Number	Rev
	SKL-Y CPU (DD/EDP)	A
Date:	Friday, August 28, 2015	Sheet 2 of 48







Security Flash Descriptors

4/10 del R11274

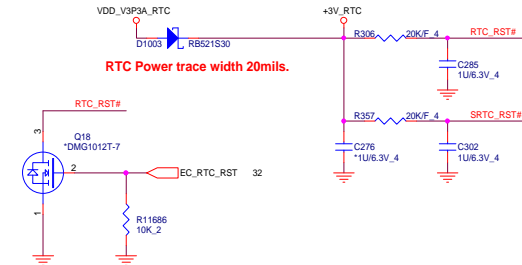
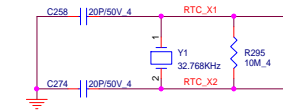
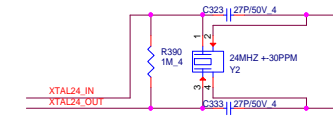
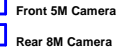
32 GPIO33_EC R11647 1K/F 2 HDA_SDOUT_R

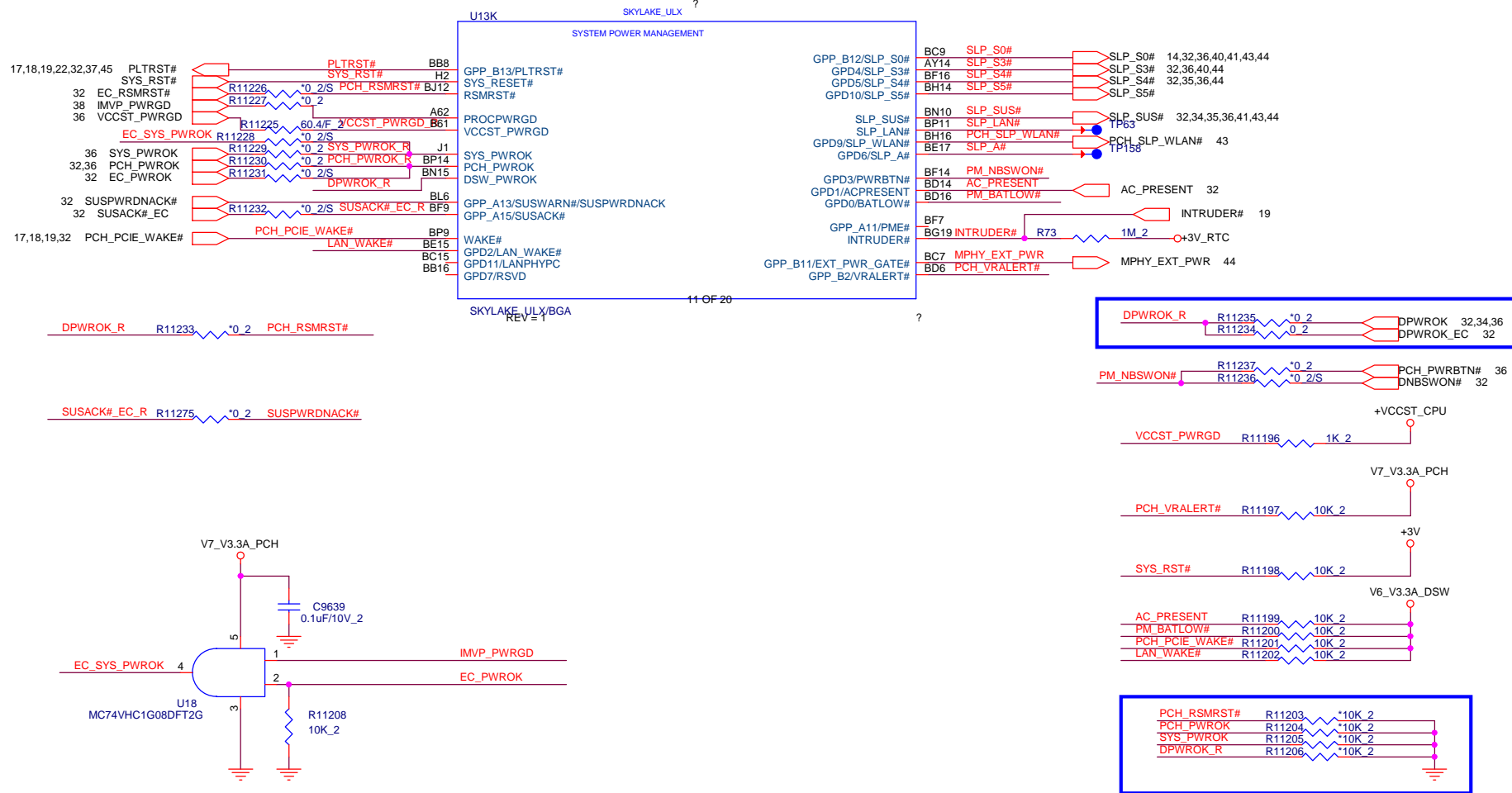
4/2 del Q7129 / add R11647



PROJECT : Millhone
Quanta Computer Inc.

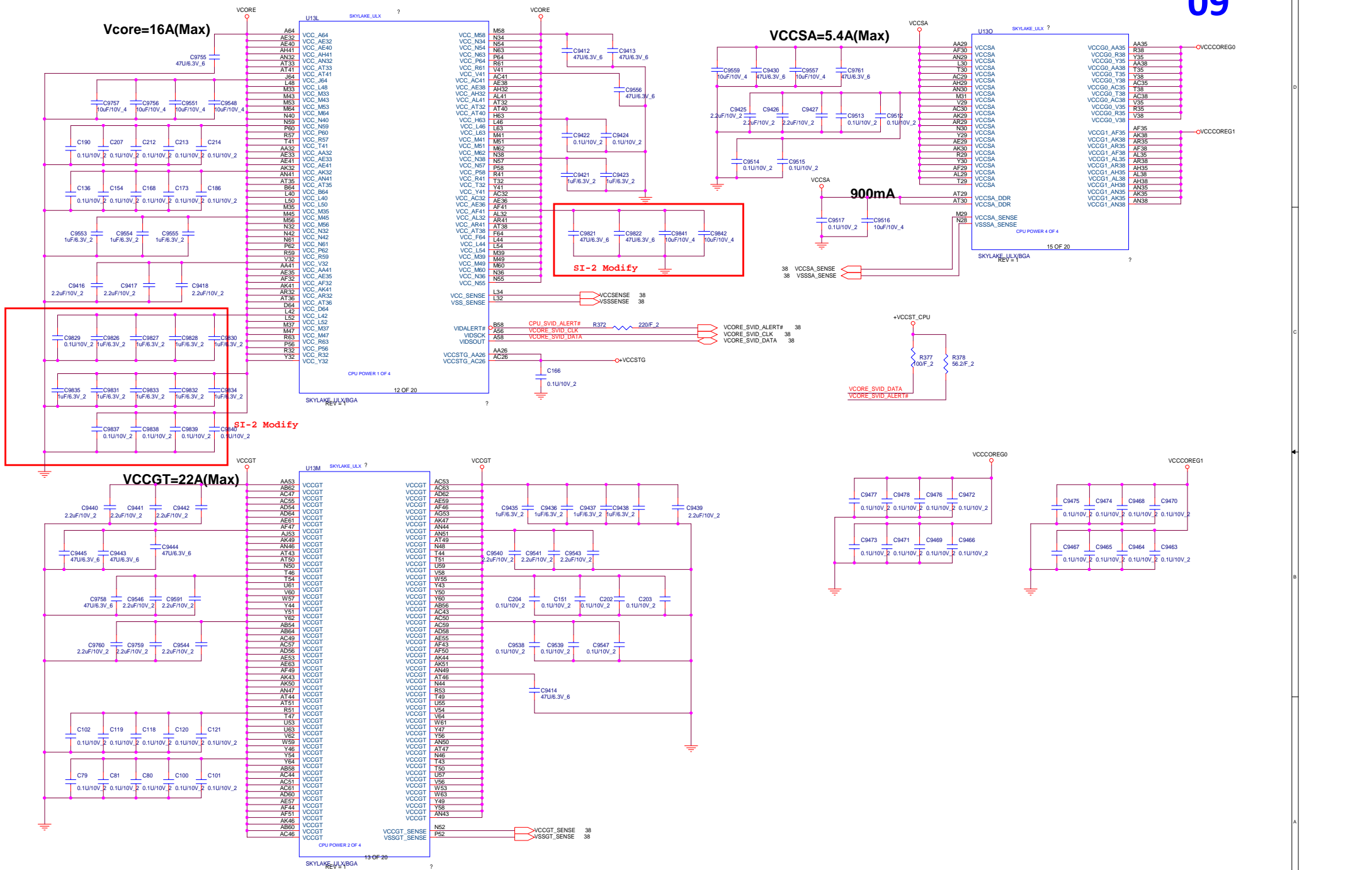
Size	Document Number	Rev
	SKL-Y CPU (LPSS/ISH/HDA)	A
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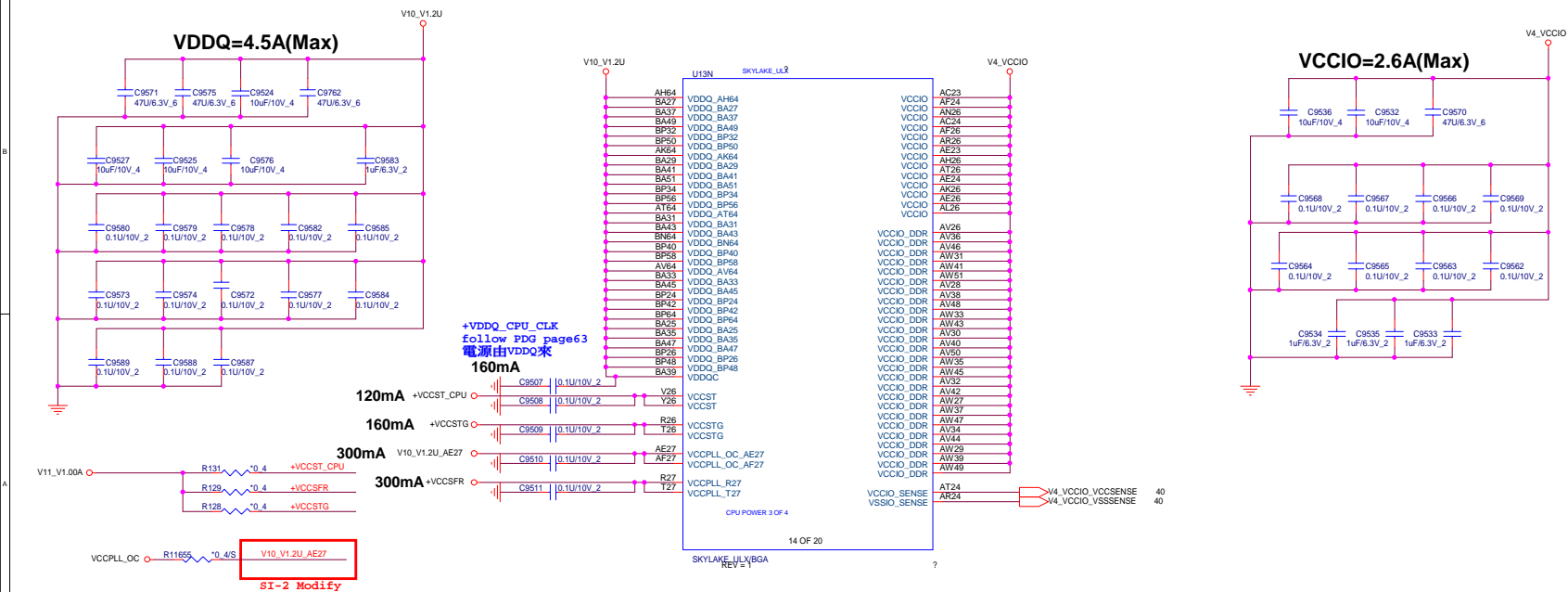
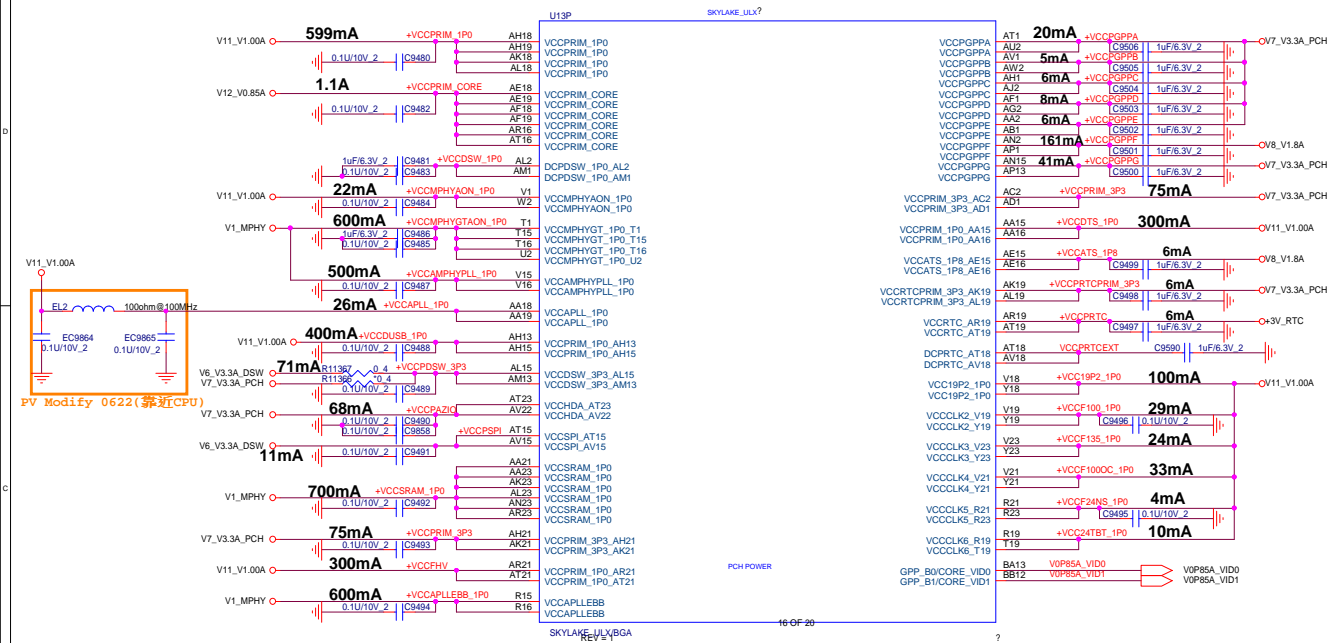




PROJECT : Millhone
Quanta Computer Inc.

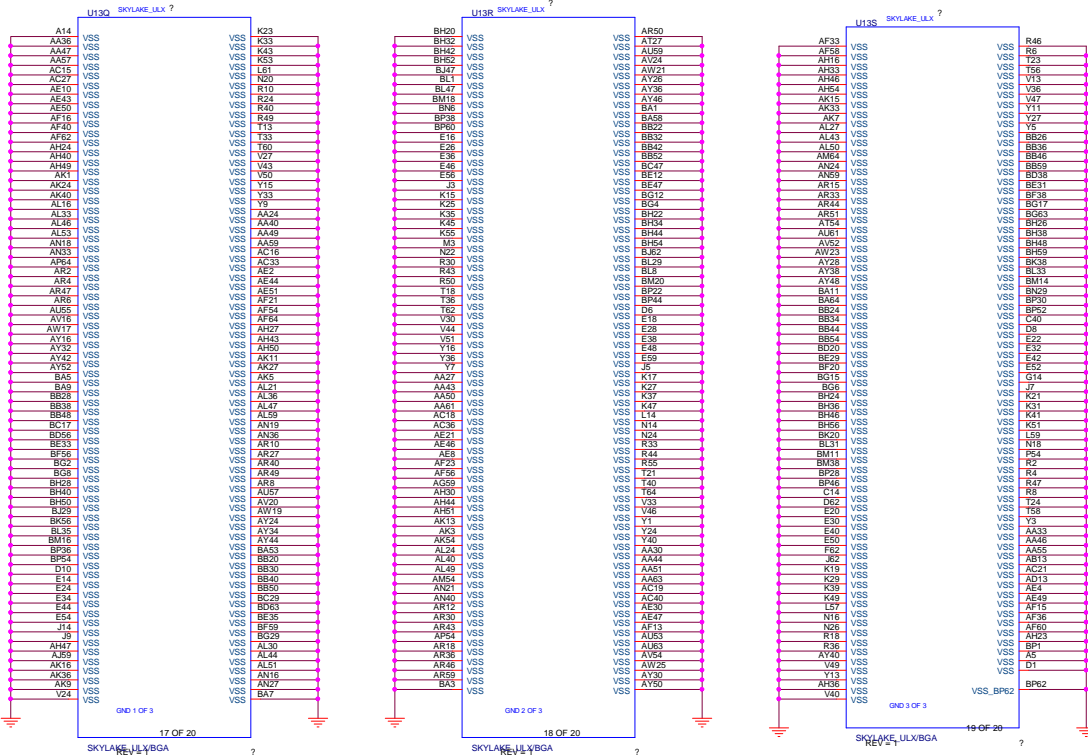
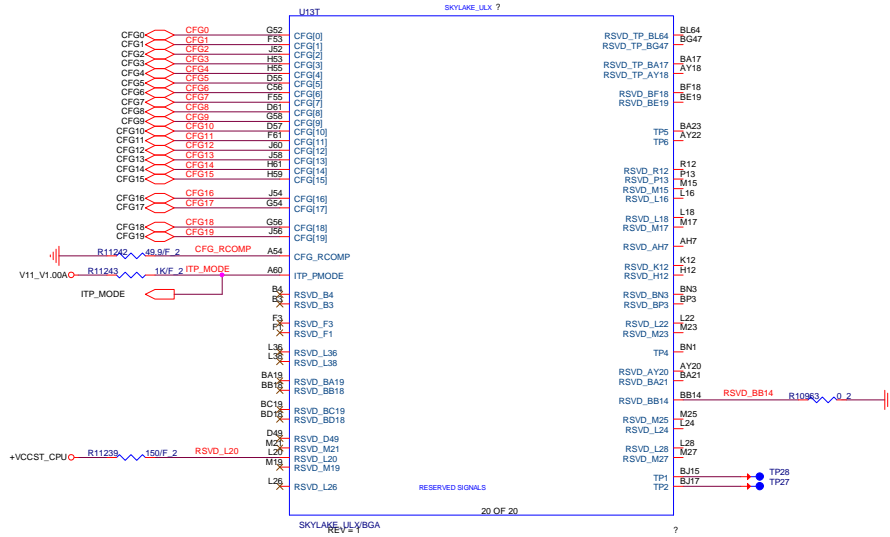
Size	Document Number	Rev
	SKL-Y CPU (PWR MANAGE)	A
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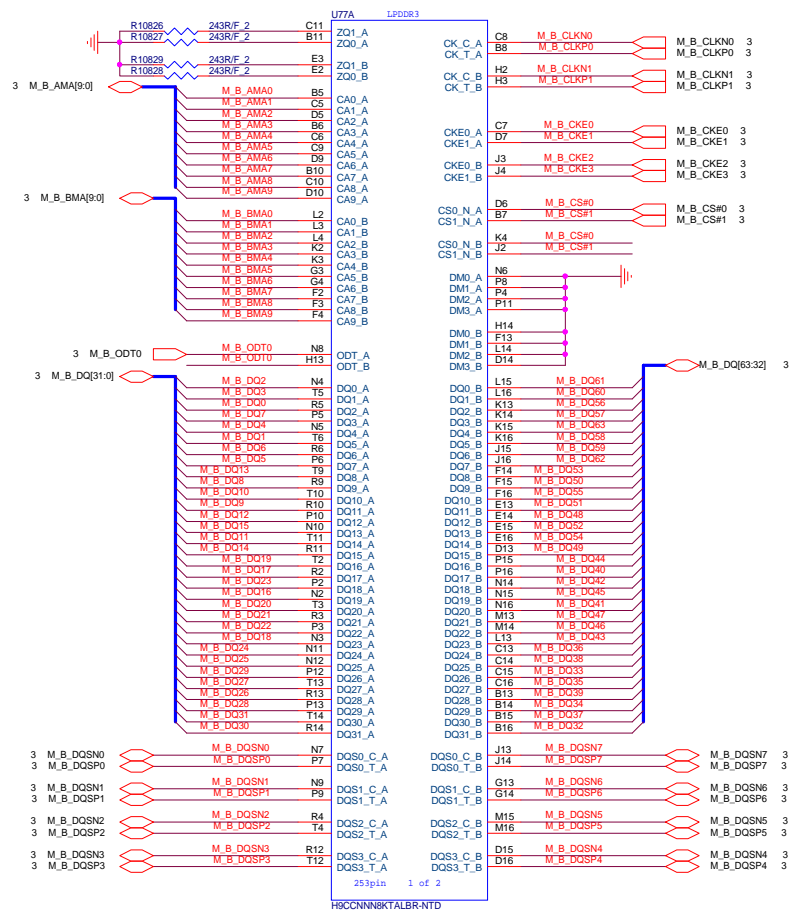
Processor Strapping

	1	0	
CFG4 eDP Enable	DISABLED	ENABLED	CFG4 R11268 1K/F 2
SPKR / GPP_B14	ENABLED	DISABLED	5.20 AC2_SPK R11279 10K 2 +3V
GPIO0 MOSI /GPP_B16	ENABLED	DISABLED	5 No_Reboot R11271 10K 2 +3V
SMBALERT# /GPP_C2	ENABLED	DISABLED	Already Pull-high on Page.4
Boot BIOS Strap Bit /GPP_B22	LPC	SPI	(default:SPI)
SML0ALERT# / GPP_C5	ESPI	LPC	Already Pull-high on Page.4(default:LPC)
SML1ALERT# / PCHHOT# GPP_B23			Already Pull-high on Page.6
SPI0_MOSI			Already Pull-high on Page.4
SPI0_MISO			Already Pull-high on Page.4
SPI0_IO2			Already Pull-high on Page.4
SPI0_IO3			Already Pull-high on Page.4
HDA_SDO/ I2S_TXDD	DISABLED	ENABLED	Already Pull-high on Page.5
Security Flash Descriptors			
DDPB_CTRLDATA /GPP_E19	ENABLED		Already Pull-high on Page.2
DDPC_CTRLDATA /GPP_E21	ENABLED		Already Pull-high on Page.2

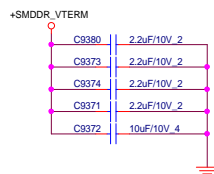








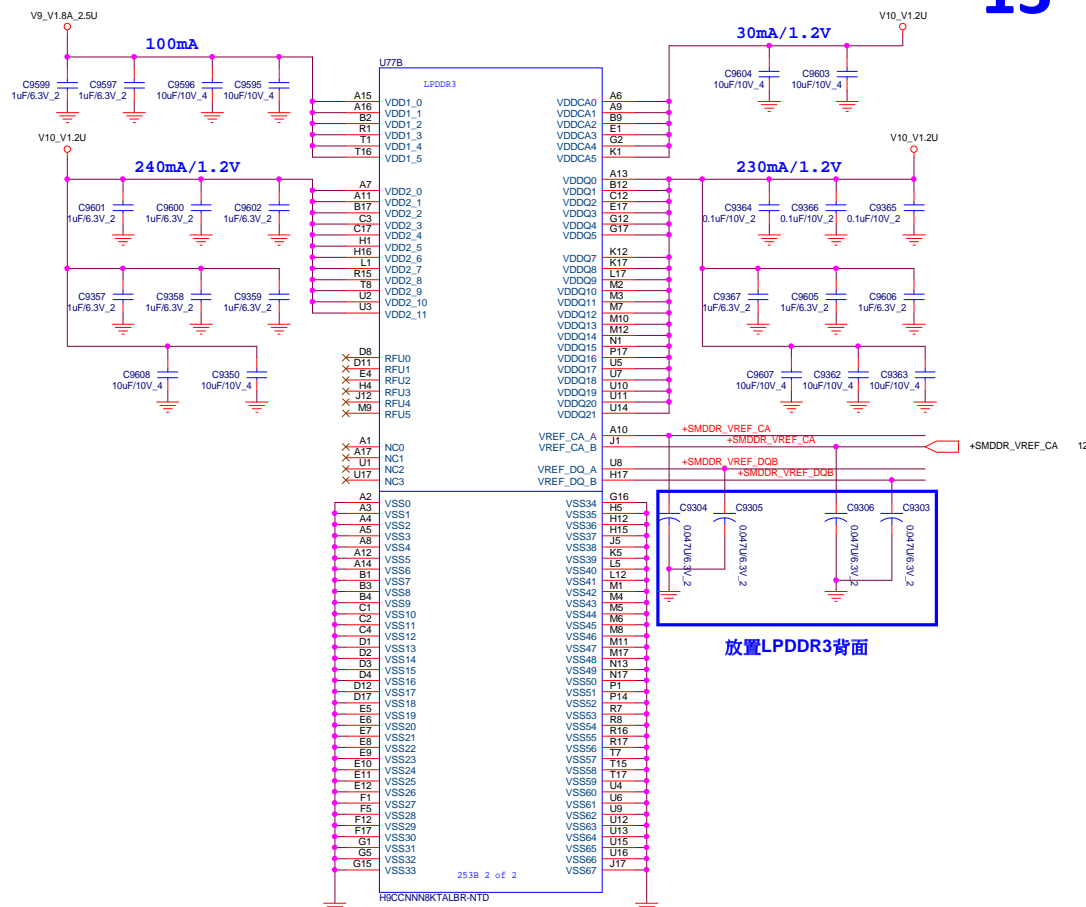
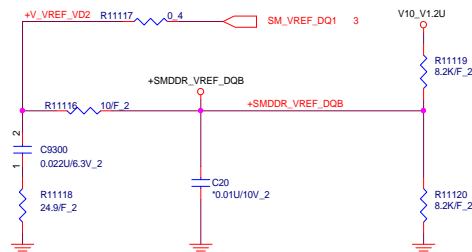
SI-2 Modify
:delete the VTT termination
(CTRL , CKE ,CMD ,CLK)

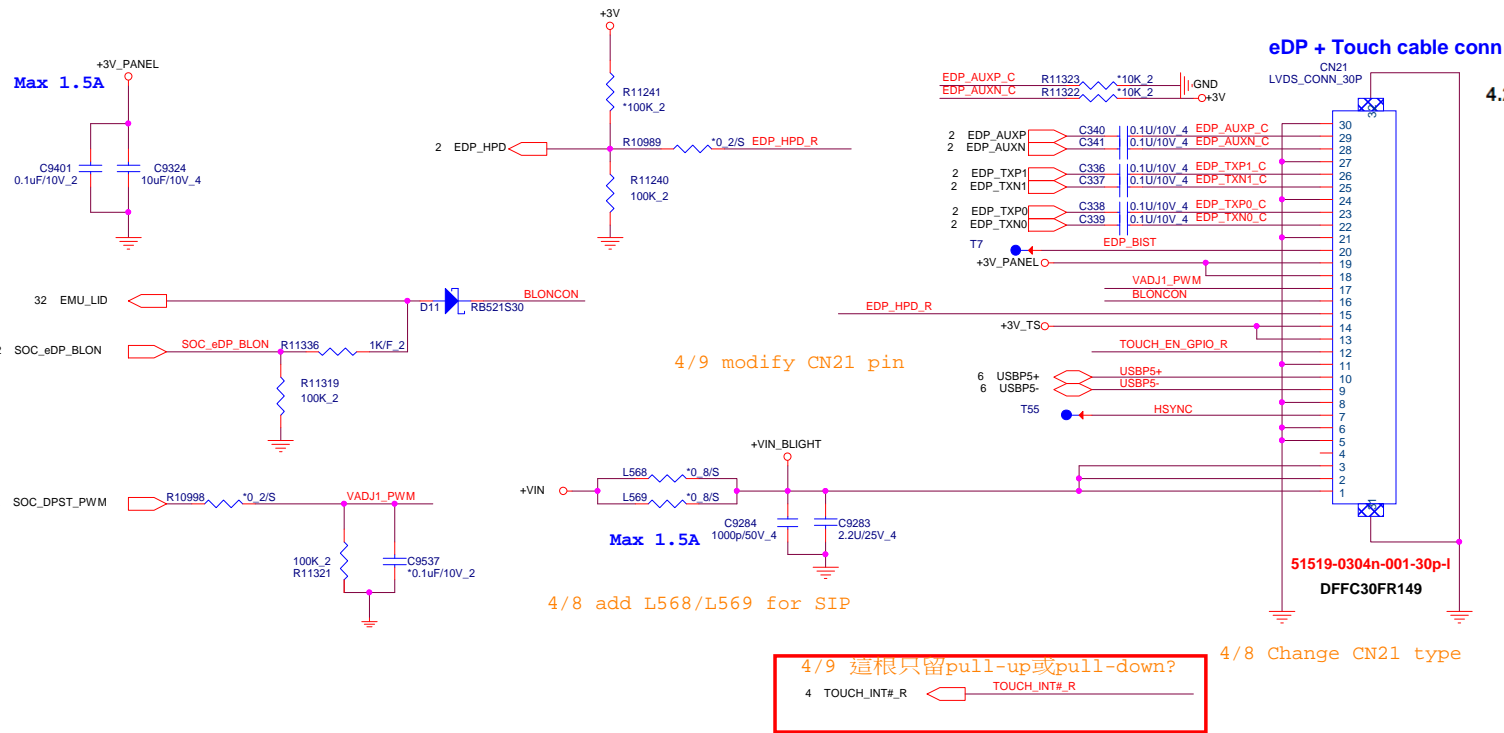


+SMDDR_VTERM 12.35

M3 VREF

M1 VREF

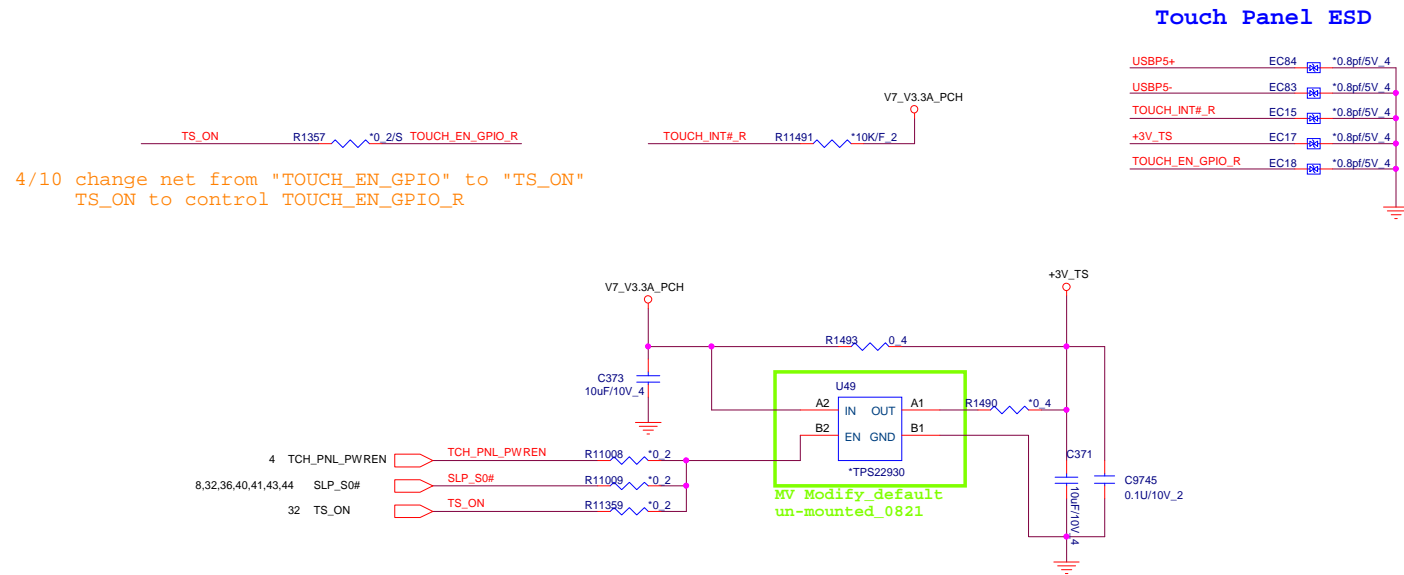


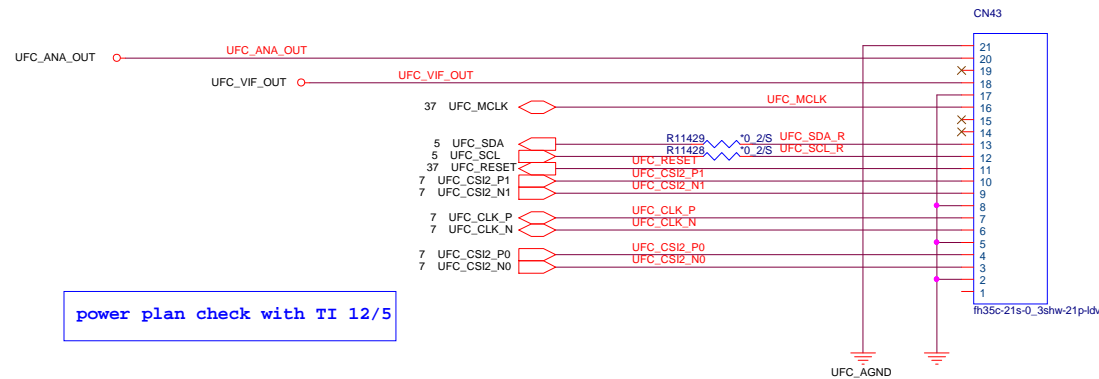
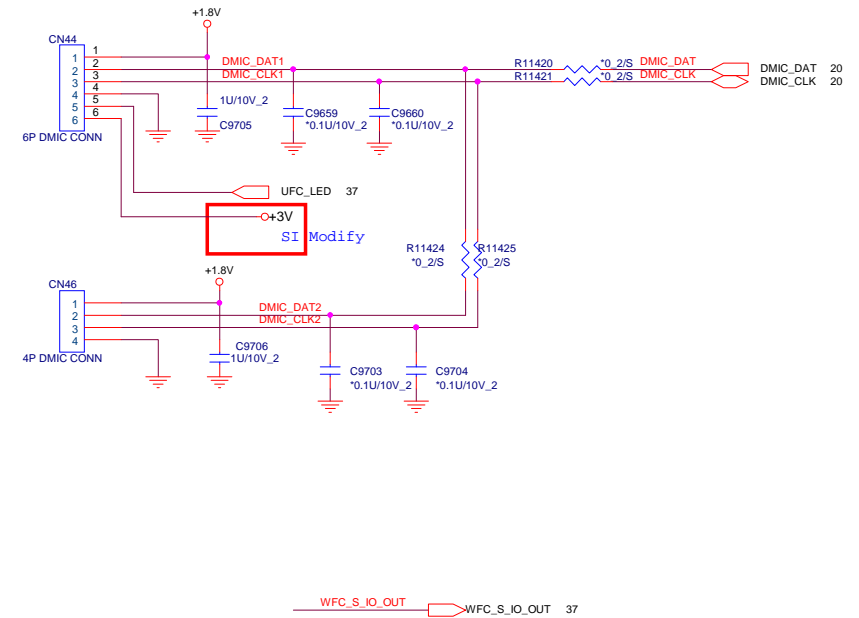
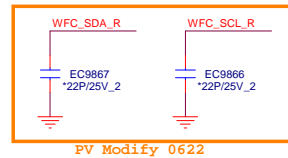


4.2. INTERFACE CONNECTIONS

PIN ASSIGNMENT

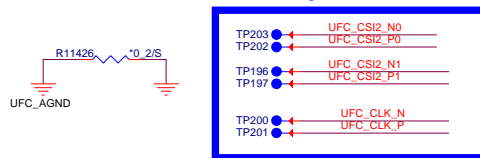
Pin	Symbol	Description
1	NC	No Connection (Reserved)
2	H_GND	High Speed Ground
3	LANE1_N	Complement Signal Link Lane 1
4	LANE1_P	True Signal Link Lane 1
5	H_GND	High Speed Ground
6	LANE0_N	Complement Signal Link Lane 0
7	LANE0_P	True Signal Link Lane 0
8	H_GND	High Speed Ground
9	AUX_CH_P	True Signal Auxiliary Channel
10	AUX_CH_N	Complement Signal Auxiliary Channel
11	H_GND	High Speed Ground
12	VCCS	Power Supply +3.3 V (typical)
13	VCCS	Power Supply +3.3 V (typical)
14	BIST	LCD Panel Self Test Enable
15	GND	Ground
16	GND	Ground
17	HPD	Hot Plug Detect
18	BL_GND	Backlight Ground
19	BL_GND	Backlight Ground
20	BL_GND	Backlight Ground
21	BL_GND	Backlight Ground
22	LED_EN	Backlight Enable Signal of LED Converter
23	LED_PWM	PWM Dimming Control Signal of LED Converter
24	NC	No Connection (Reserved)
25	NC	No Connection (Reserved)
26	LED_VCCS	Backlight Power
27	LED_VCCS	Backlight Power
28	LED_VCCS	Backlight Power
29	LED_VCCS	Backlight Power
30	NC	No Connection (Reserved)



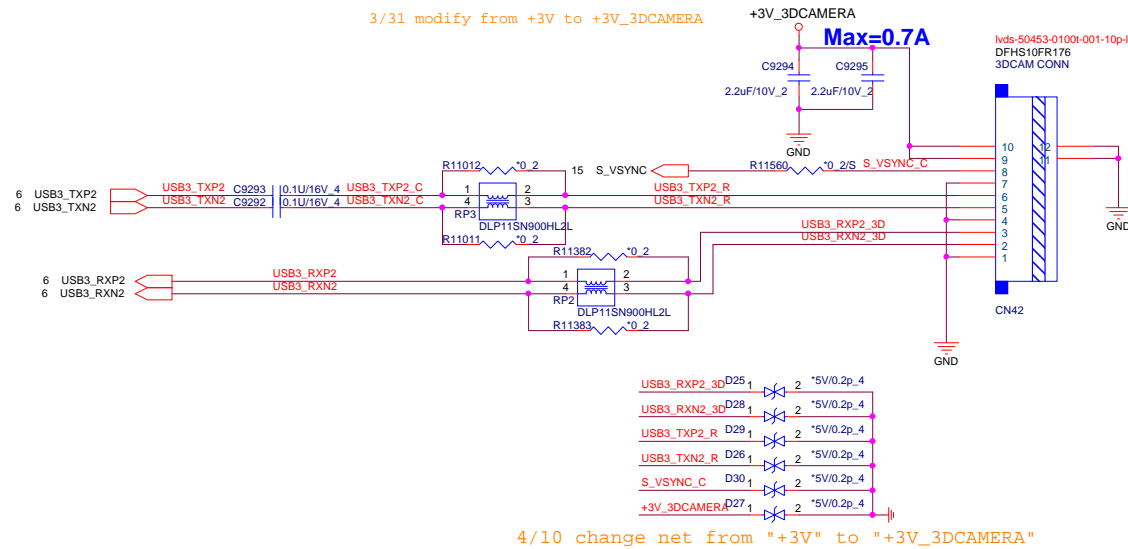



power plan check with TI 12/5

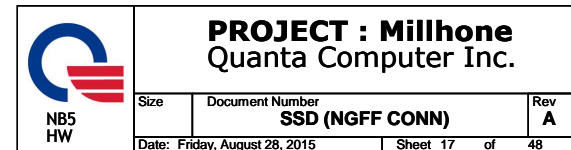
SI-2 modify Close to CN43



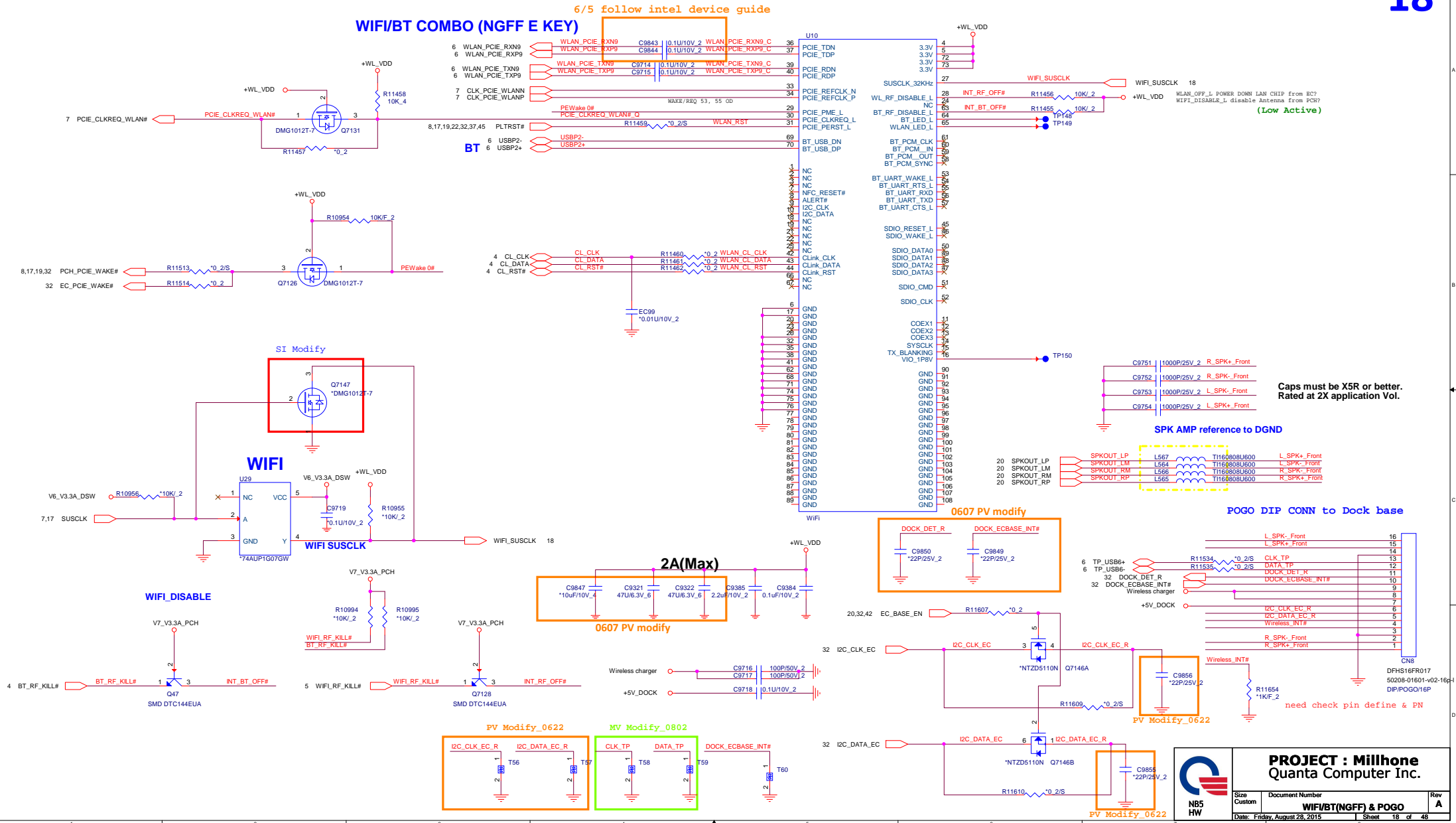
Intel R200 3D camera



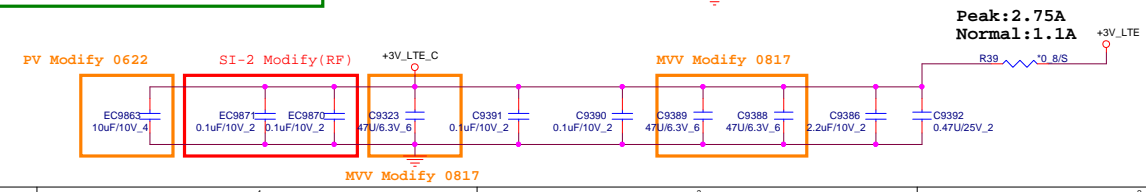
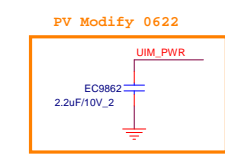
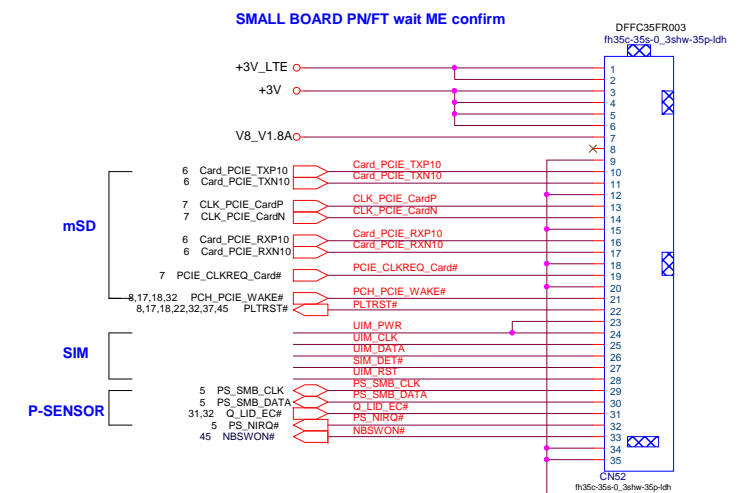
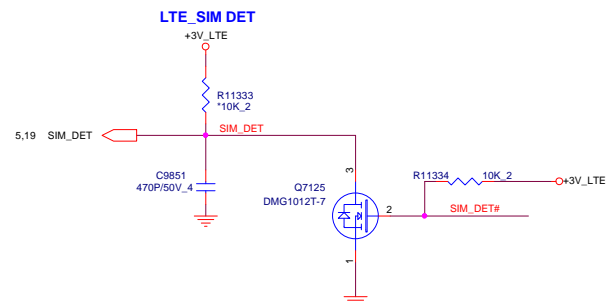
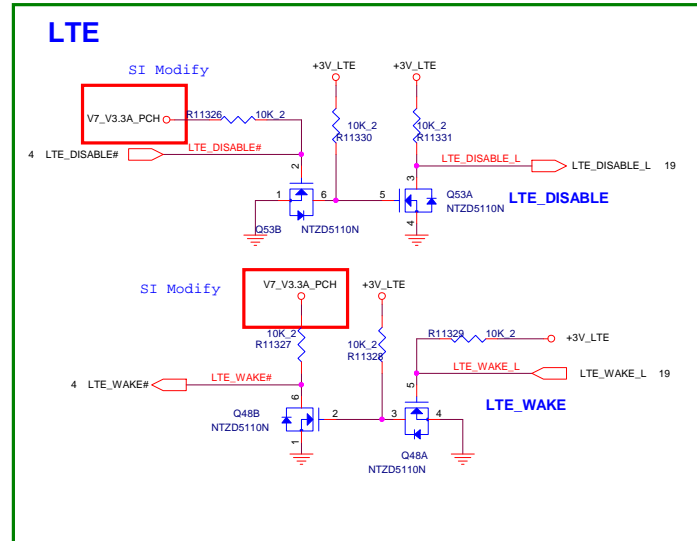
	PROJECT : Millhone		
	Quanta Computer Inc.		
	Size Custom	Document Number Intel D R200 Camera	Rev A
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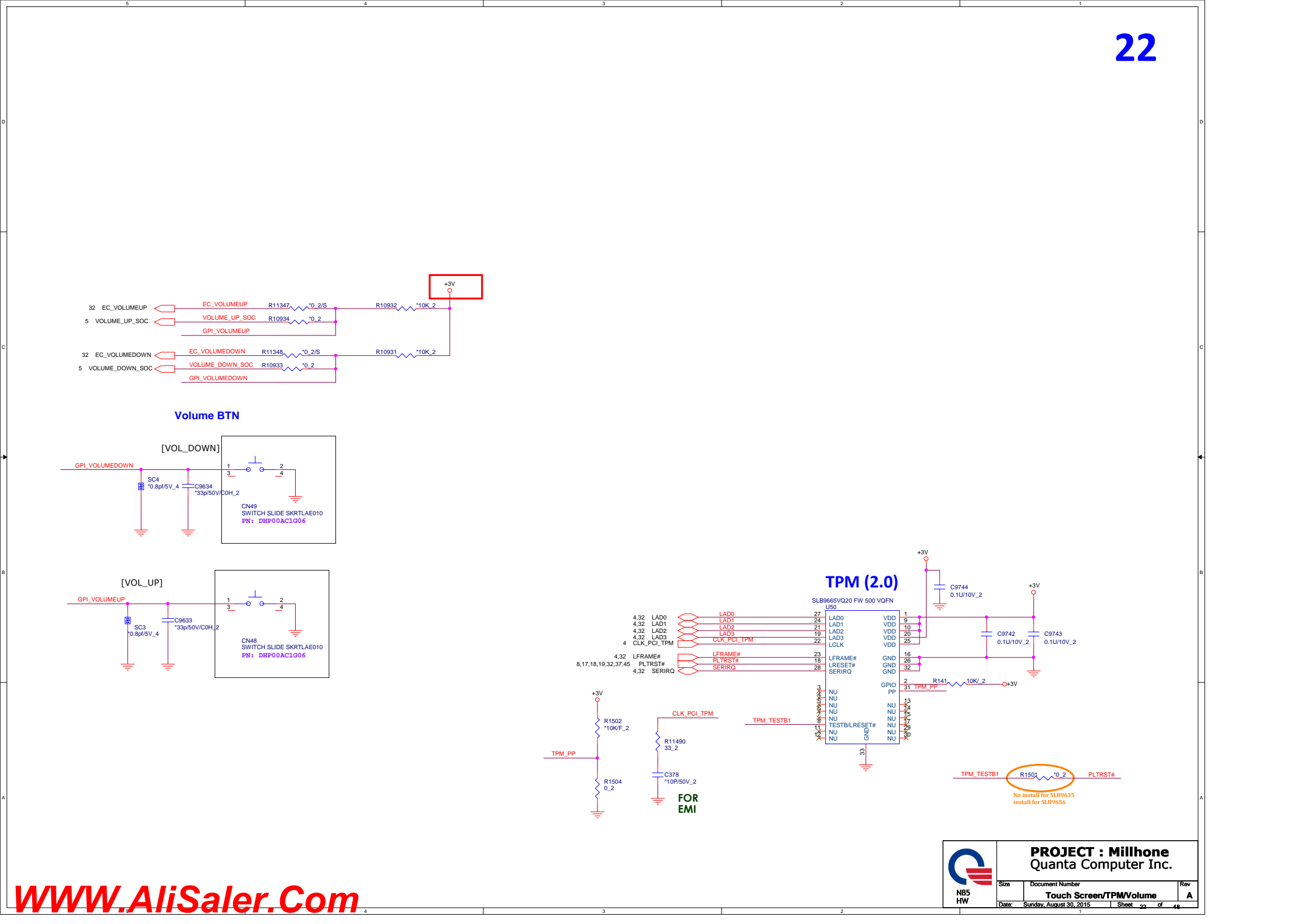
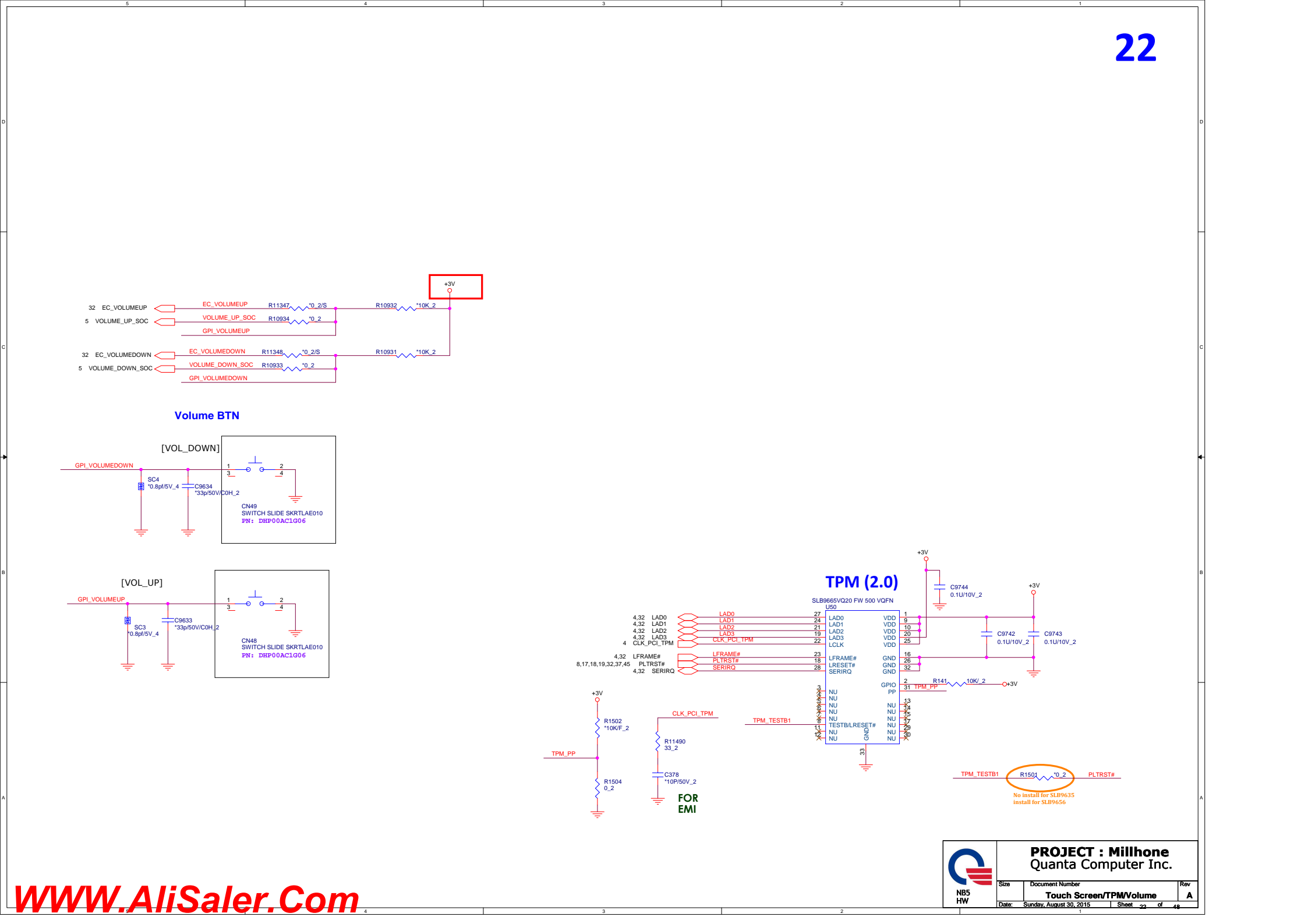
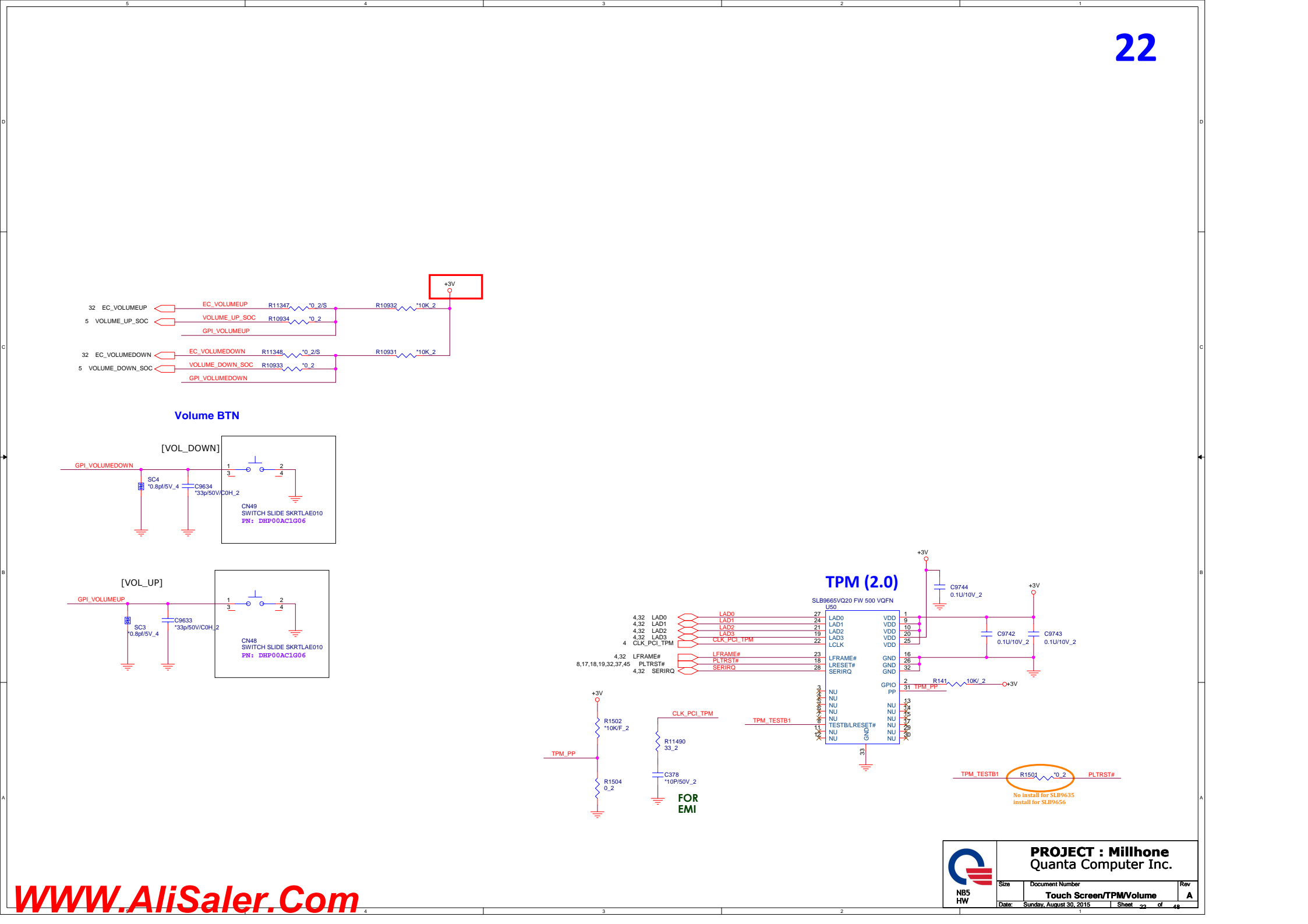
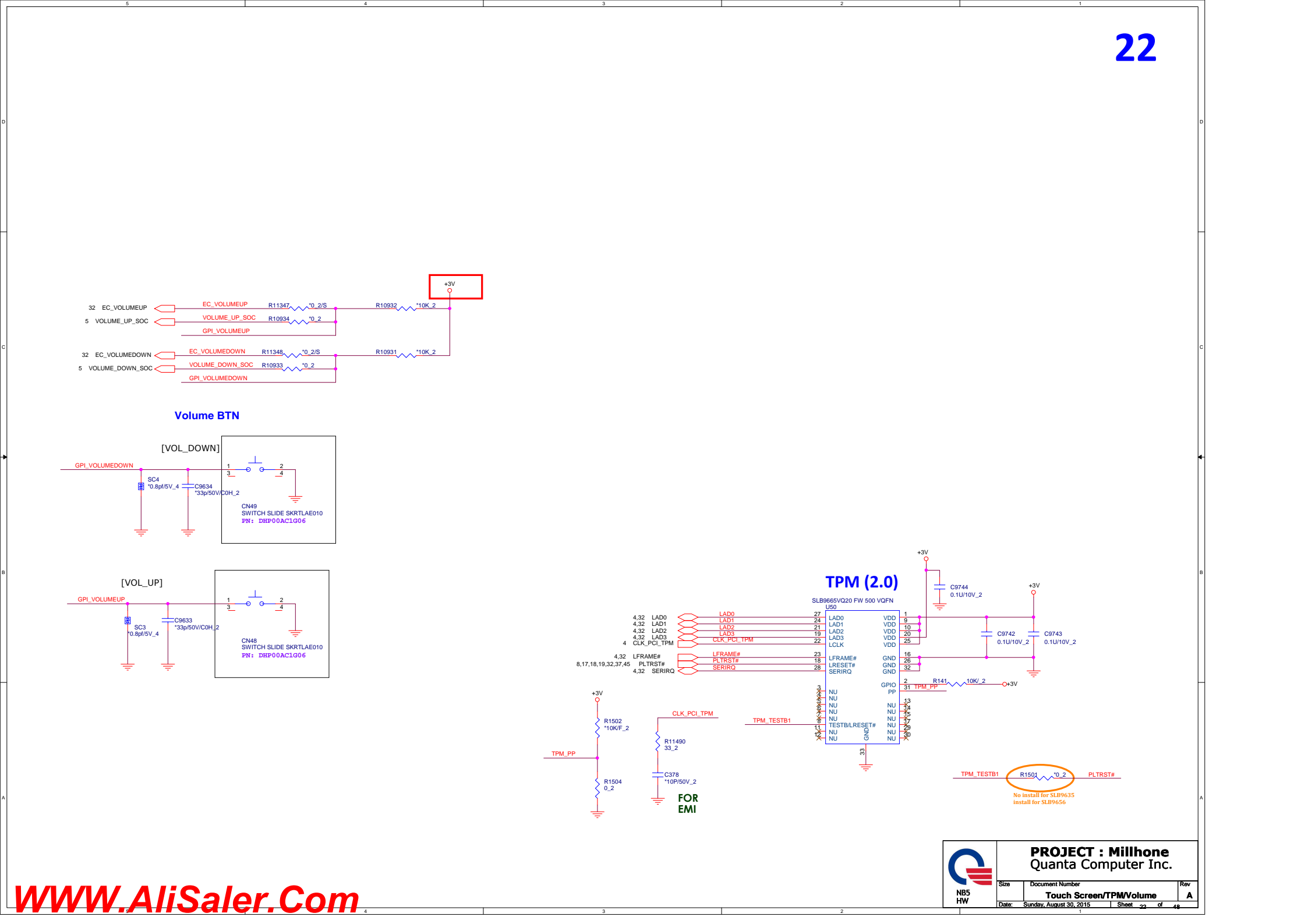
6/5 follow intel device guide

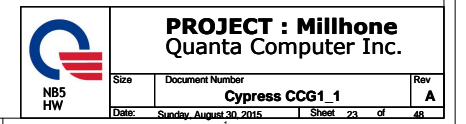


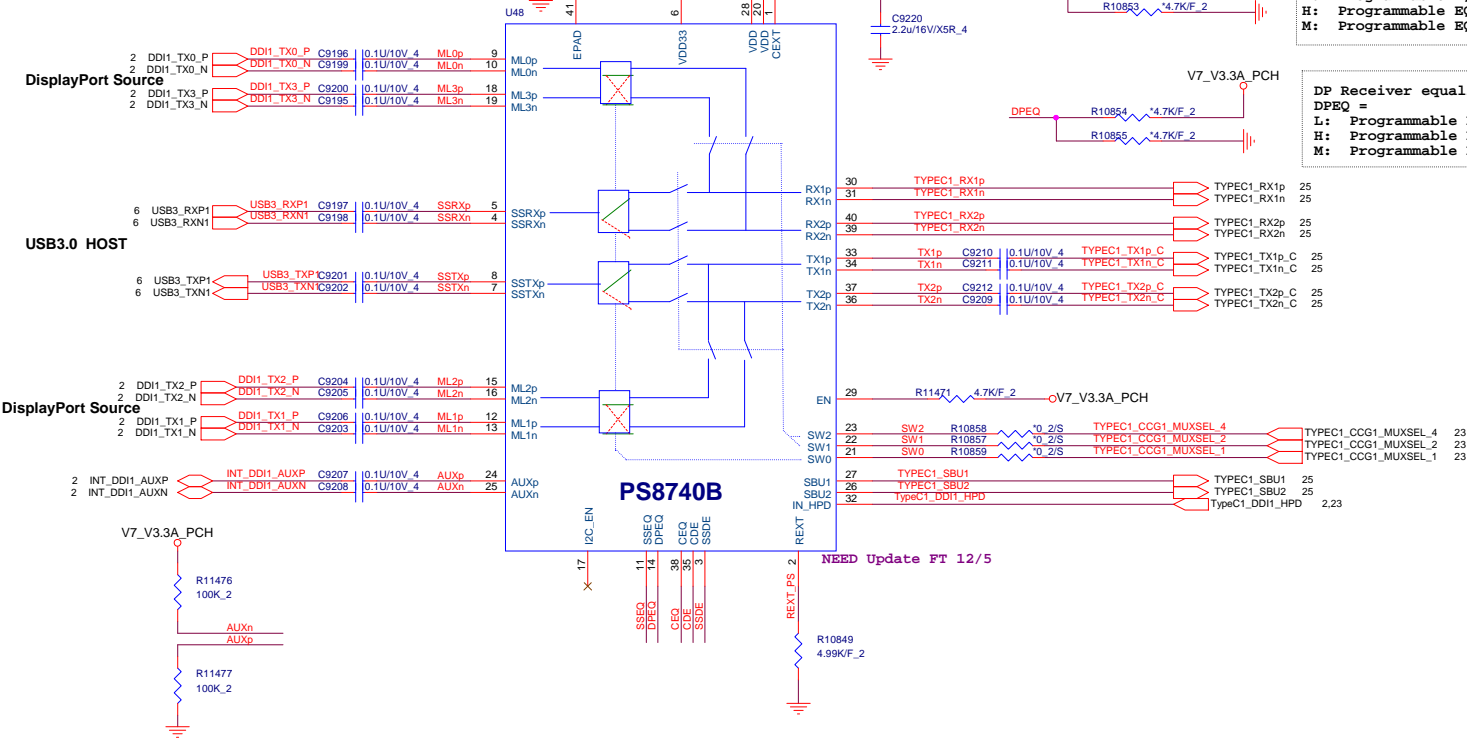
19



 NB5 HW	PROJECT : Millhone Quanta Computer Inc.		
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		NA	A
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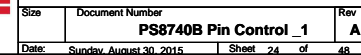
[illegible]



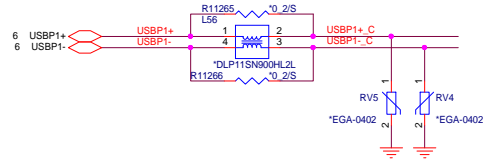


PS8740 Mode Selection			
SW2	SW1	SW0	
L	L	L	Chip Power Down
L	L	H	Chip Power Down
L	H	L	USB only on SS1 channels
L	H	H	USB only on SS2 channels
H	L	L	DP only; MLO on SRRX2
H	L	H	DP only; MLO on SRRX1
H	H	L	USB+2lanes DP; DP MLO on SRRX2
H	H	H	USB+2lanes DP; DP MLO on SRRX1

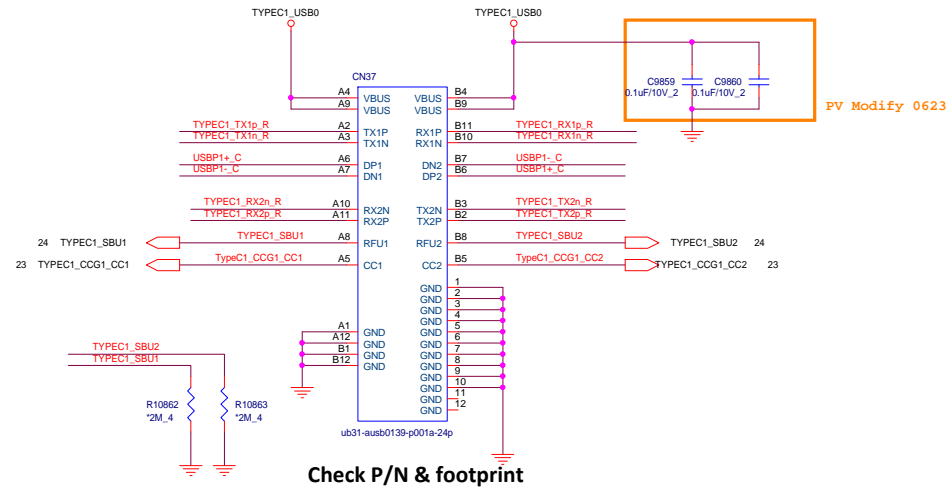
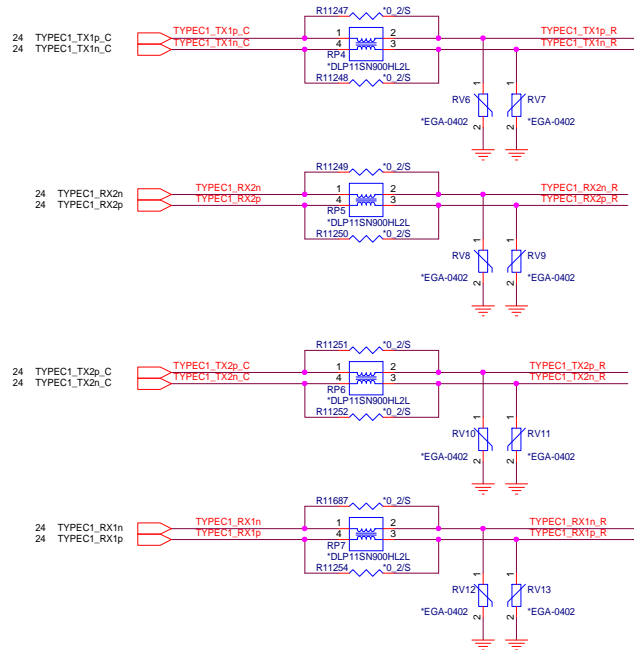
PS8740B Pin Control Mode



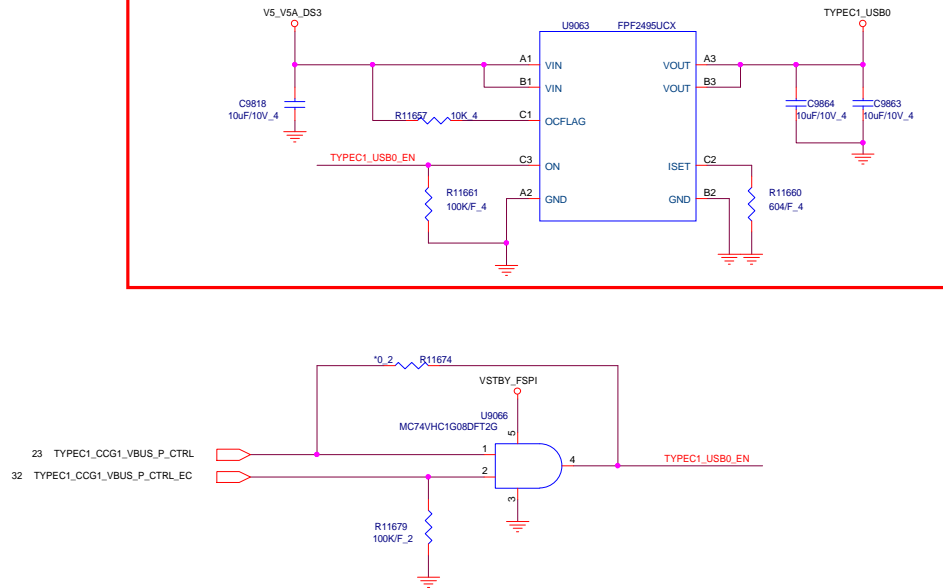
USB2.0 ESD



Type C1_HSIO_ESD



SI-2 Modify

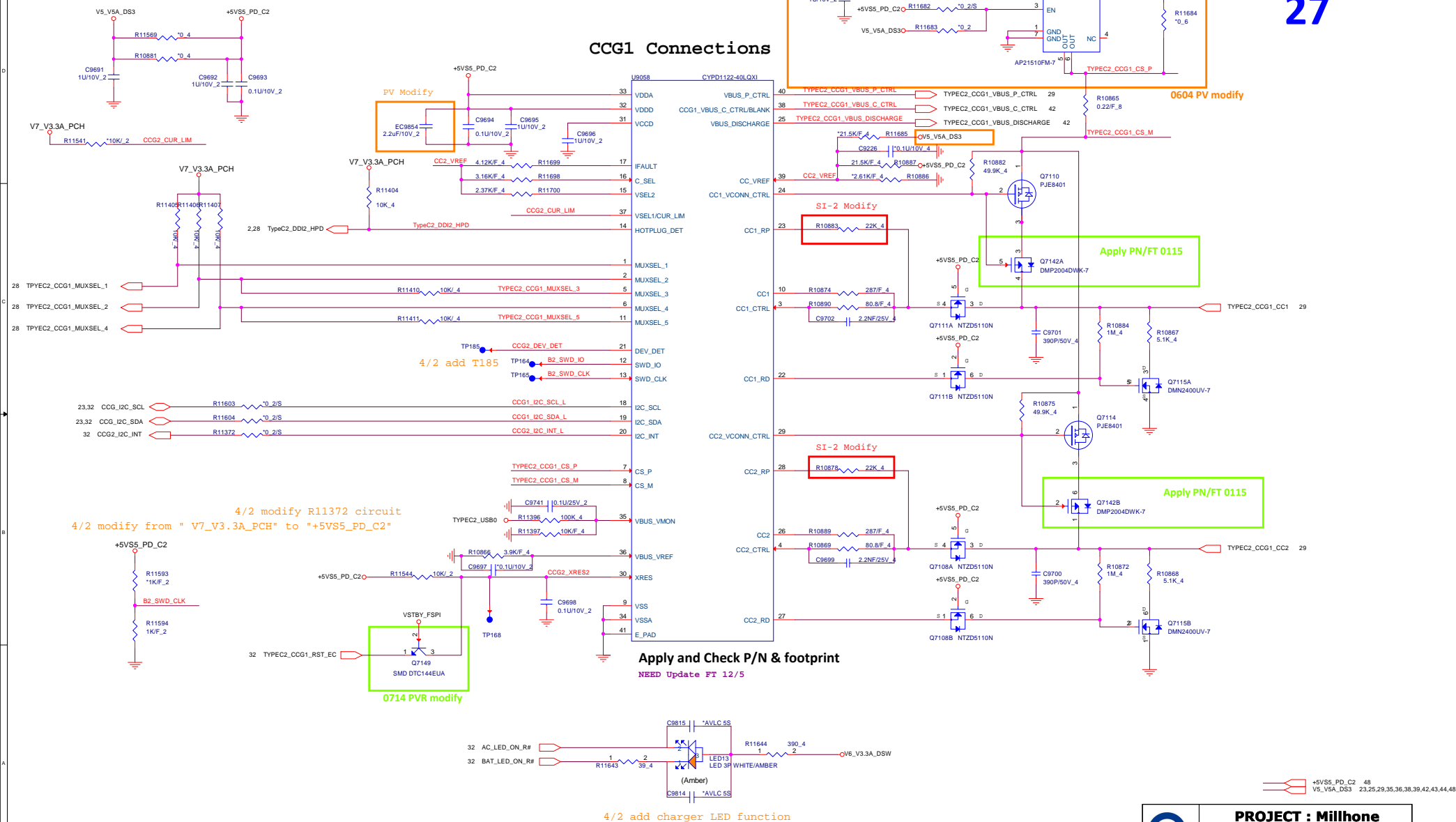




PROJECT : Millhone
Quanta Computer Inc.

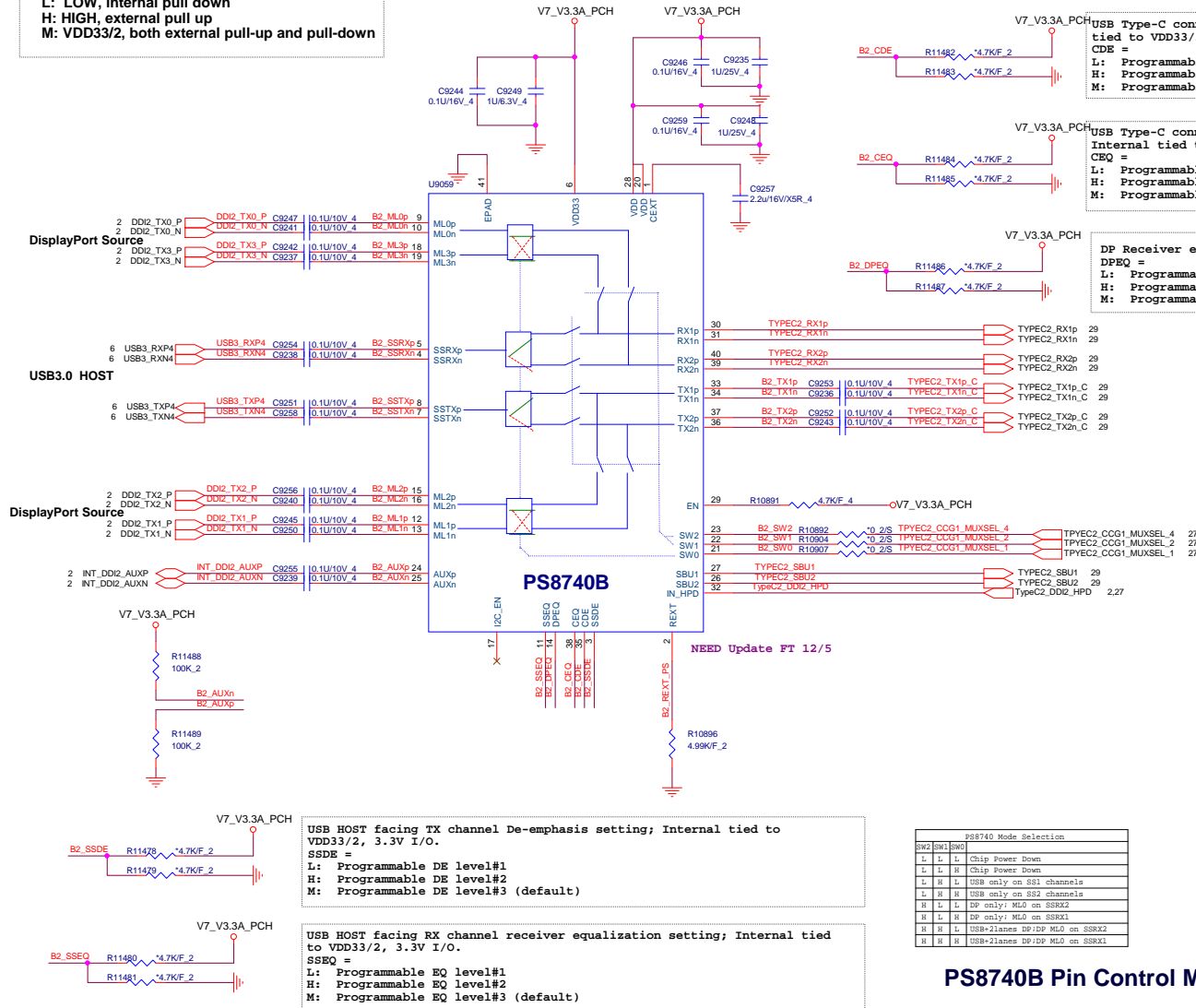
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	VBUS Provider _1	A
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CCG1 Connections



3 Level Input:

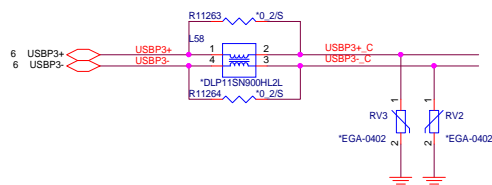
L: LOW, internal pull down
H: HIGH, external pull up
M: VDD33/2, both external pull-up and pull-down



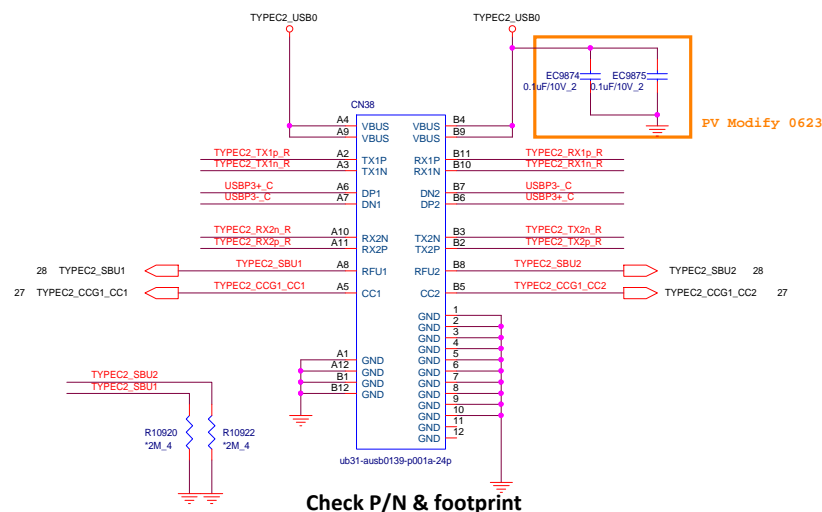
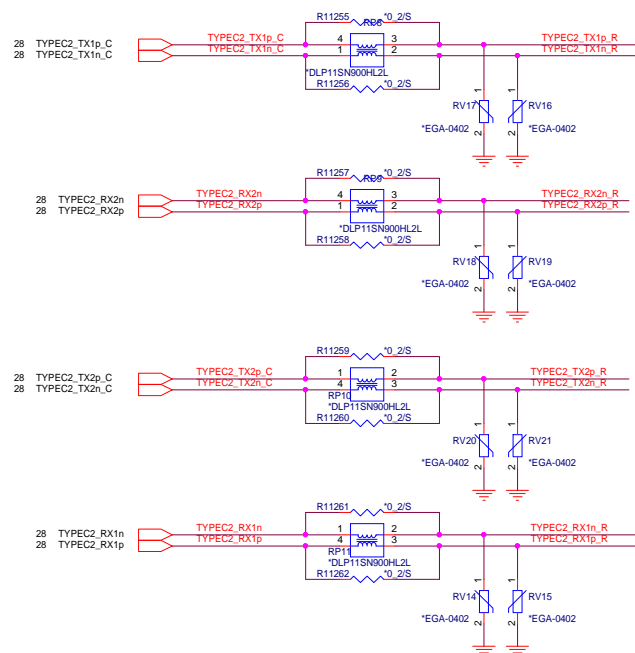
PROJECT : Millhone
Quanta Computer Inc.

Size Document Number **PS8740B Pin Control_2** Rev **A**
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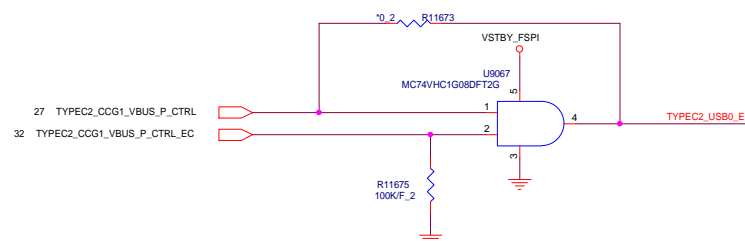
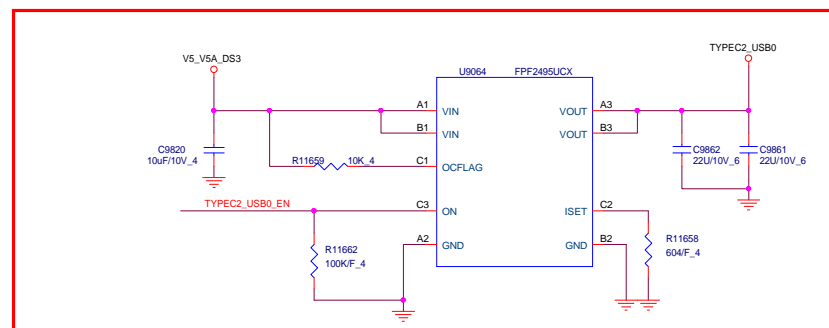
USB2.0_ESD

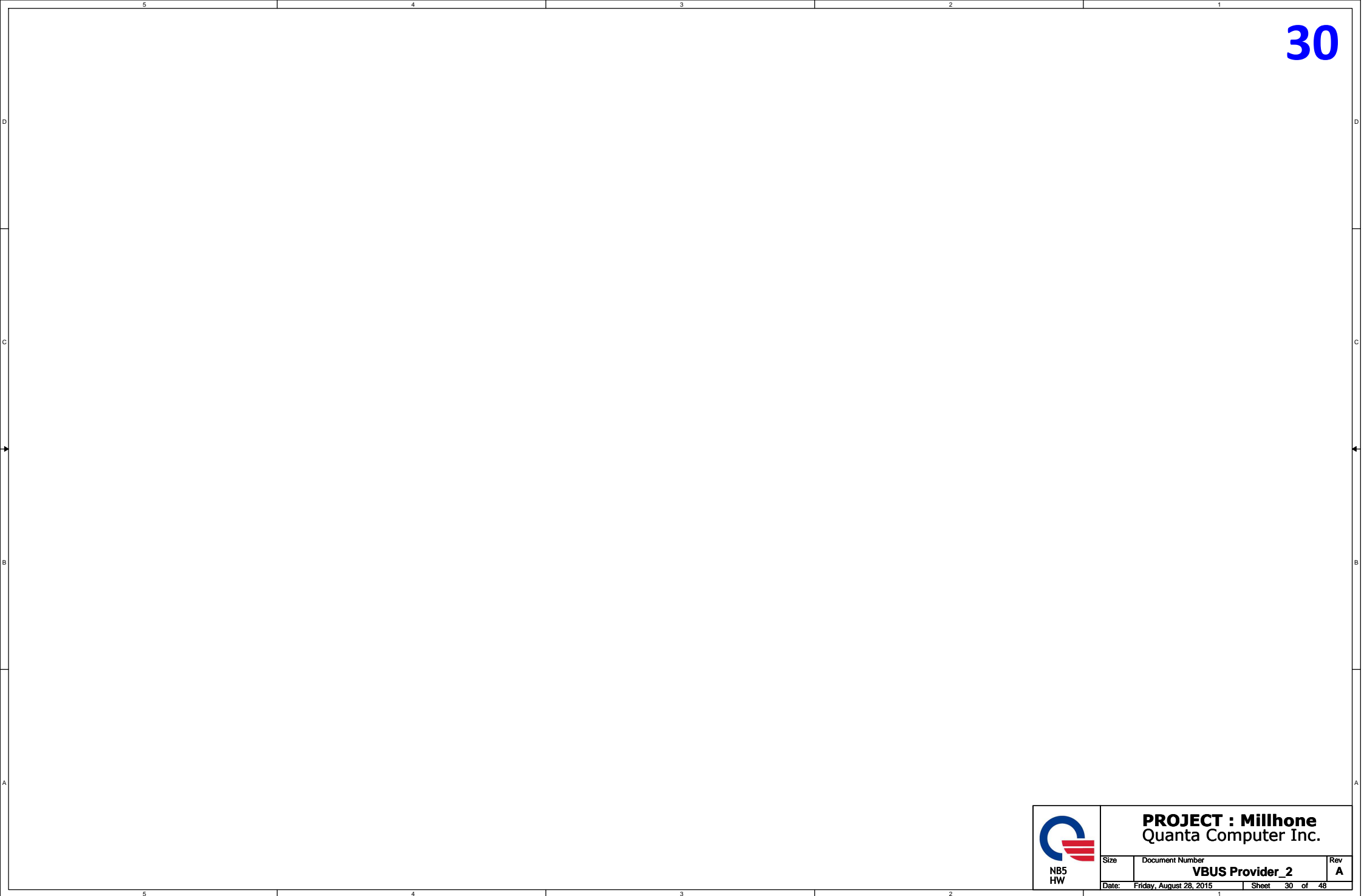



Type C2_HSIO_ESD



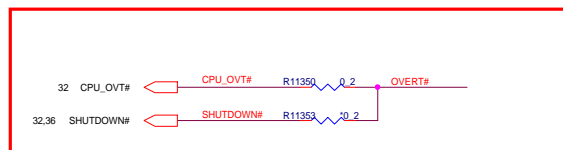
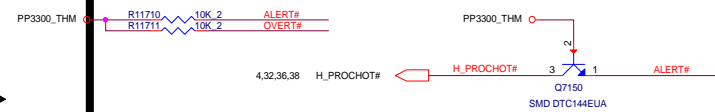
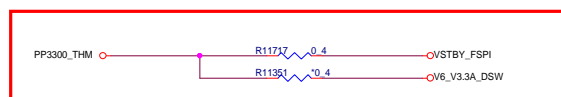
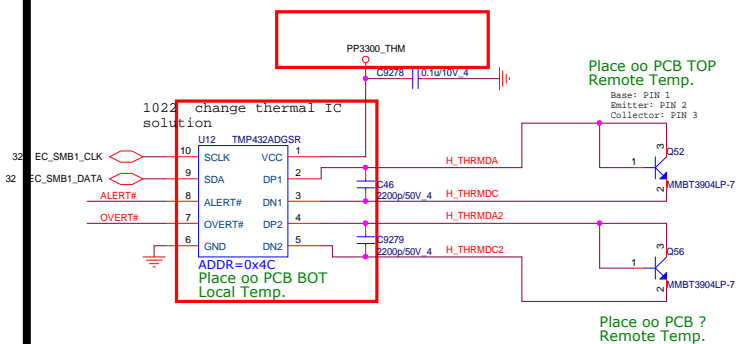
SI-2 Modify



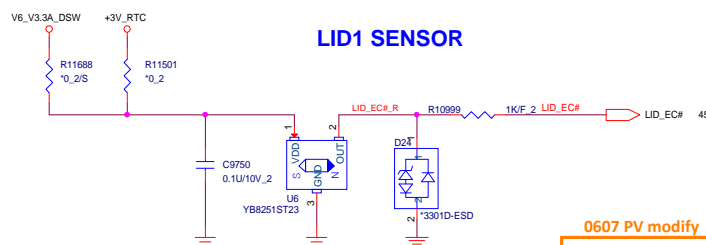


 NB5 HW	PROJECT : Millhone Quanta Computer Inc.		
	Size	Document Number	Rev
	VBUS Provider_2		A
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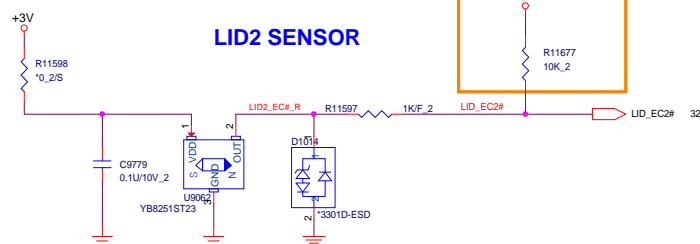
Thermal Sensor (THM)



LID1 SENSOR

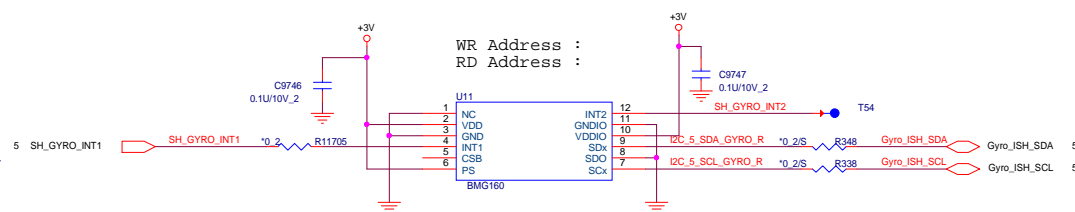


LID2 SENSOR



4/9 change net from "LID2_EC#_R" to "LID_EC#_R"

Gyroscope (BMG160)



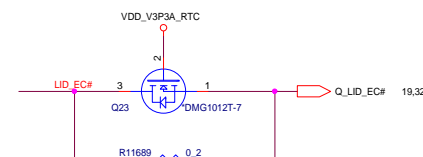
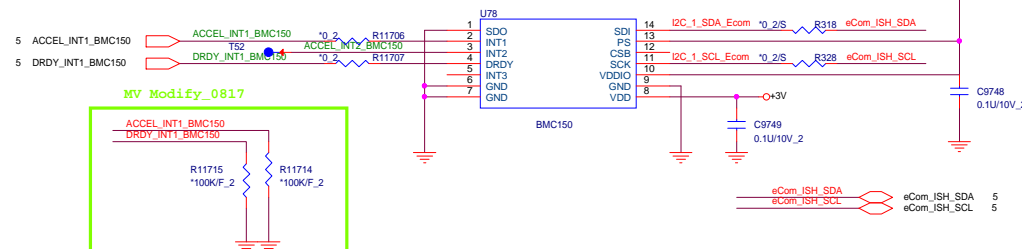
E-compass/Magnetometer/Accelerometer
(BMC150)

Keepout area is around 10mm

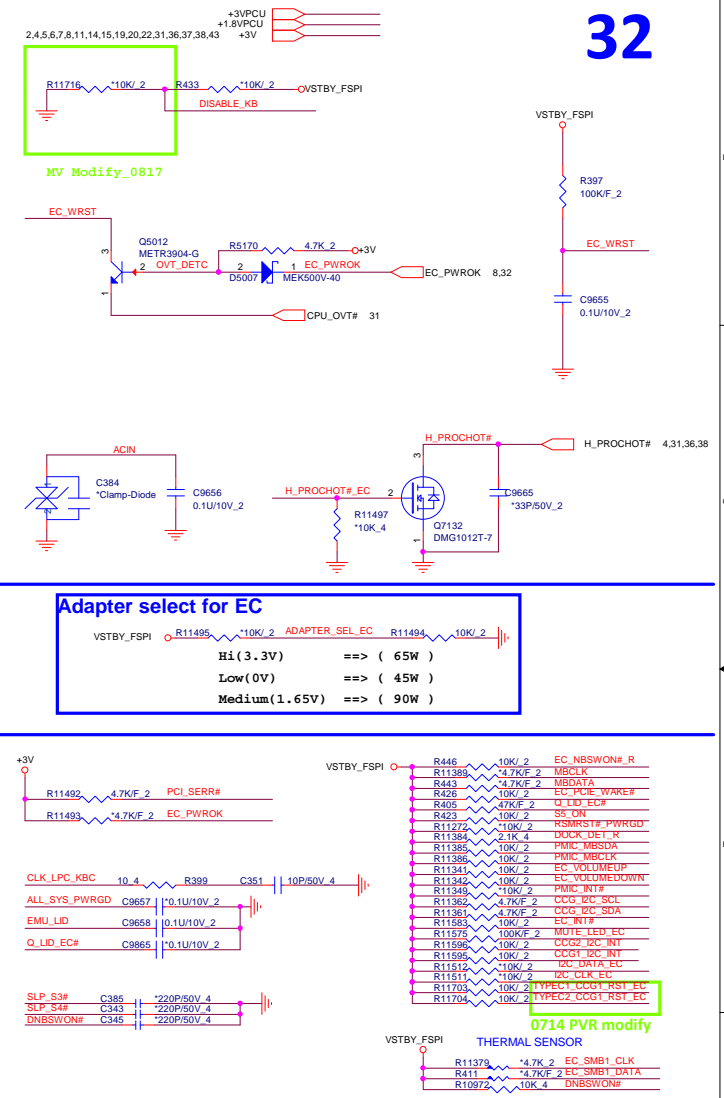
```

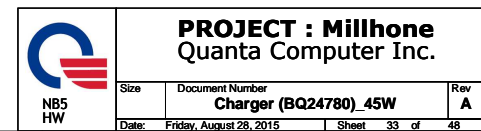
WR Address : 0x3C
RD Address : 0x3D

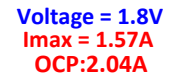
```



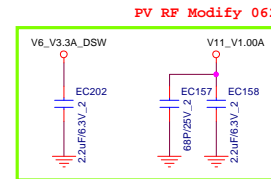
	V6_V3.3A_DSW PP3300_THM	4,8,10,18,23,27,32,34,35,36,40,41,43,48
---	----------------------------	---







Voltage = 3.3V
I_{max} = 7.5A
OCP:9.75A

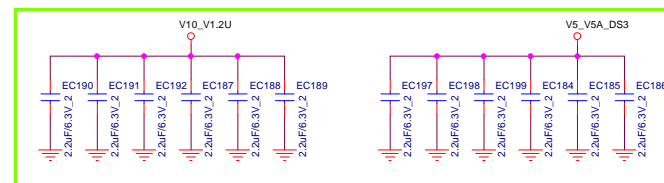
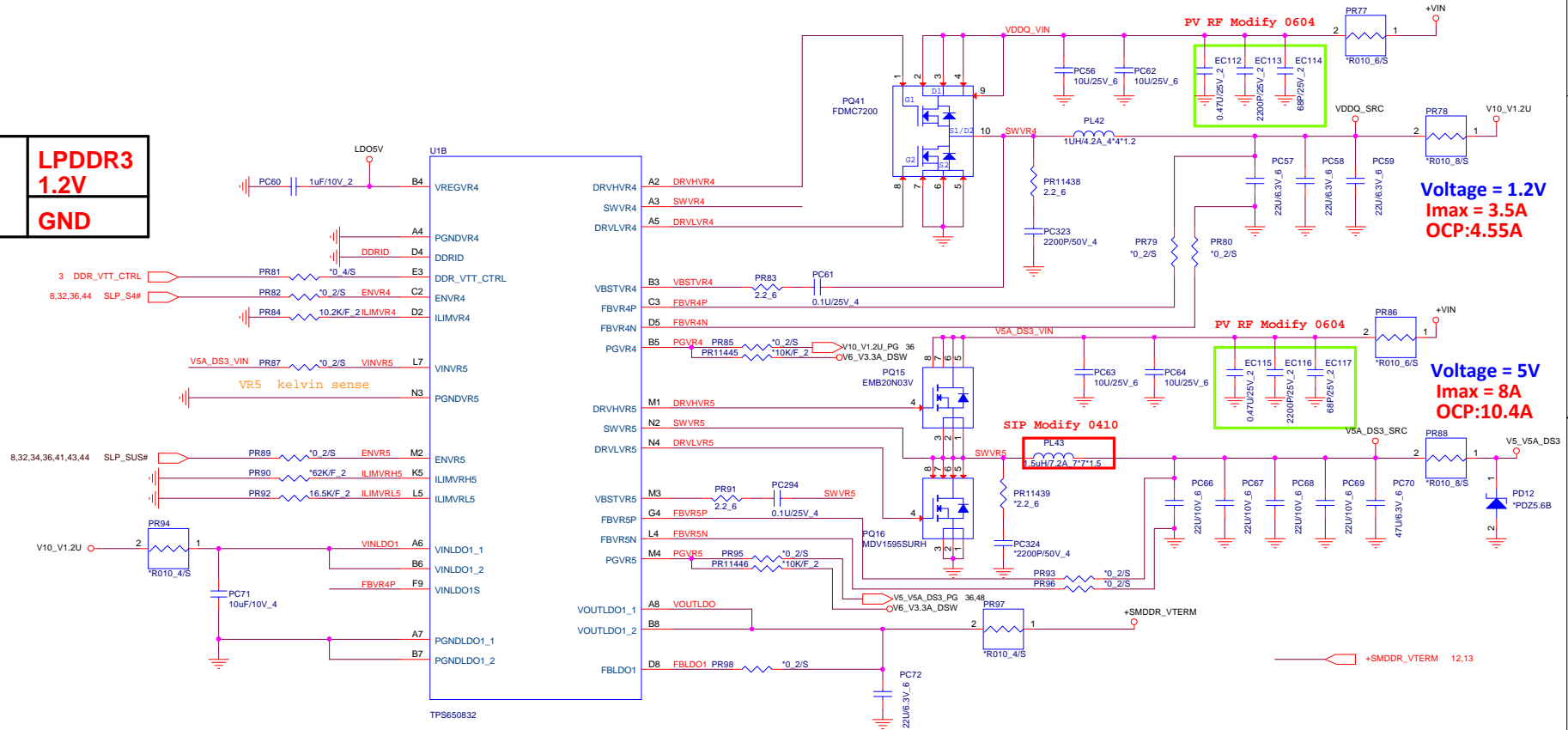


Input	Output
V6_V3.3A_DSW	V6_V3.3A_DSW
V3.3A_DSW_SRC	V3.3A_DSW_SRC
V11_V1.00A	V11_V1.00A
V1.00A_SRC	V1.00A_SRC
V8_V1.8A	V8_V1.8A
V1.8A_SRC	V1.8A_SRC



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DDRID	LPDDR3
	1.2V
	GND

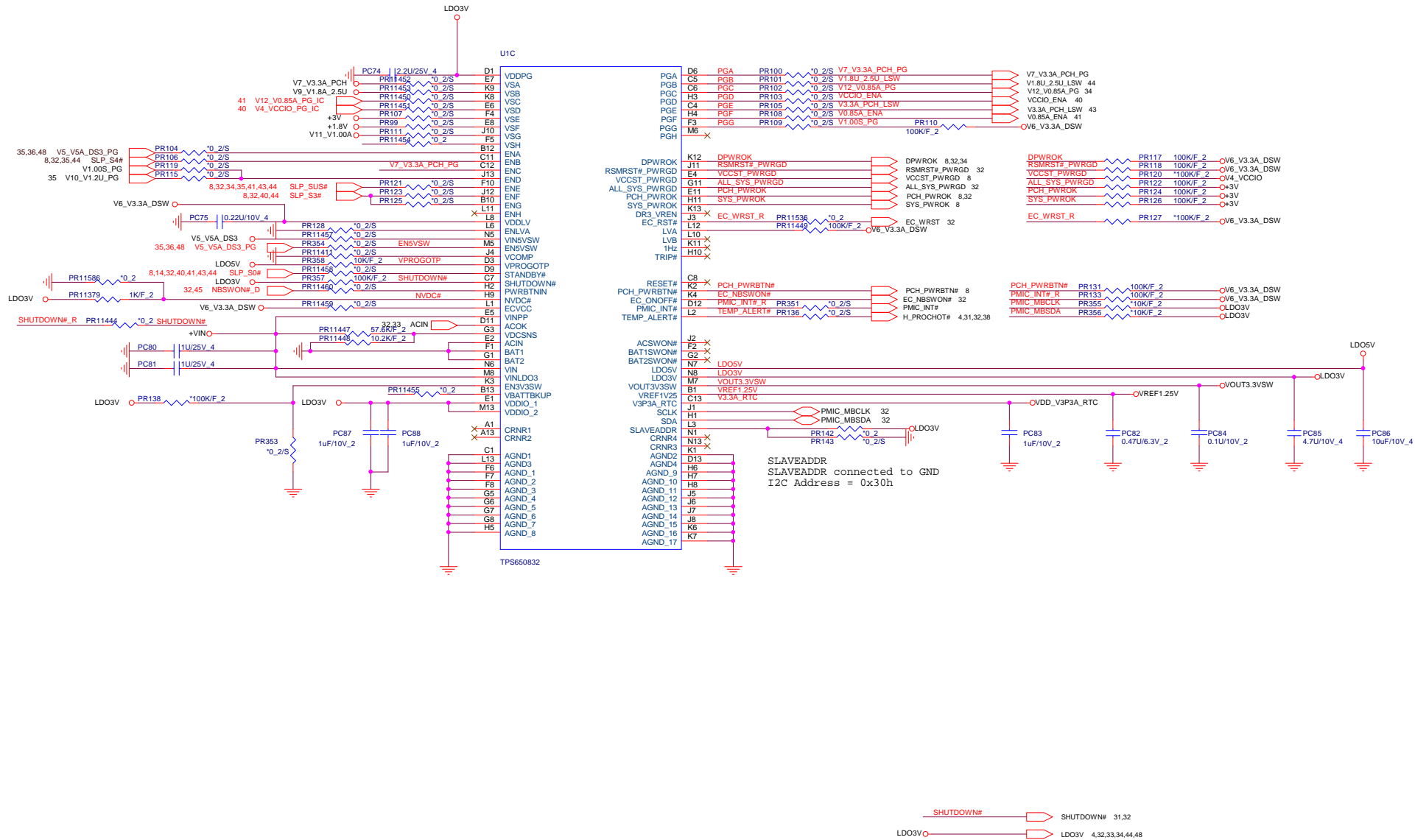


- V5_V5A_DS3 23,25,27,29,36,38,39,42,43,44,48
- V5A_DS3_SRC
- V10_V1.2U 10,12,13,44
- VDDQ_SRC
- +SMDDR_VTERM 12,13
- VOUTLDO

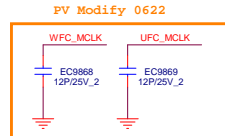
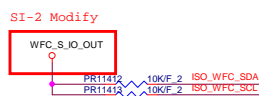


PROJECT : Millhone
Quanta Computer Inc.

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NB5 HW	System PMIC (TPS650832_2)	A
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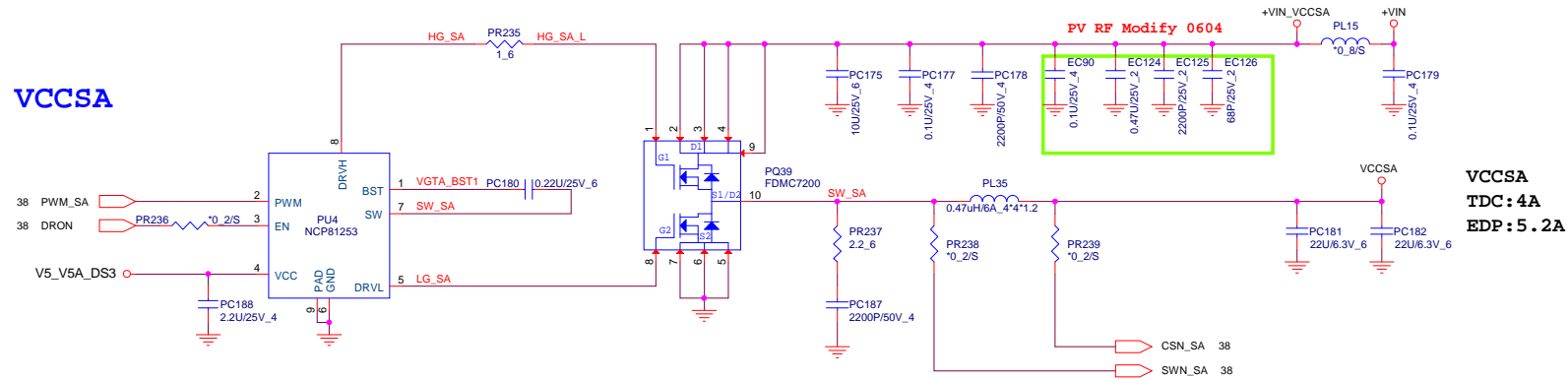


+3V 3DCAMERA



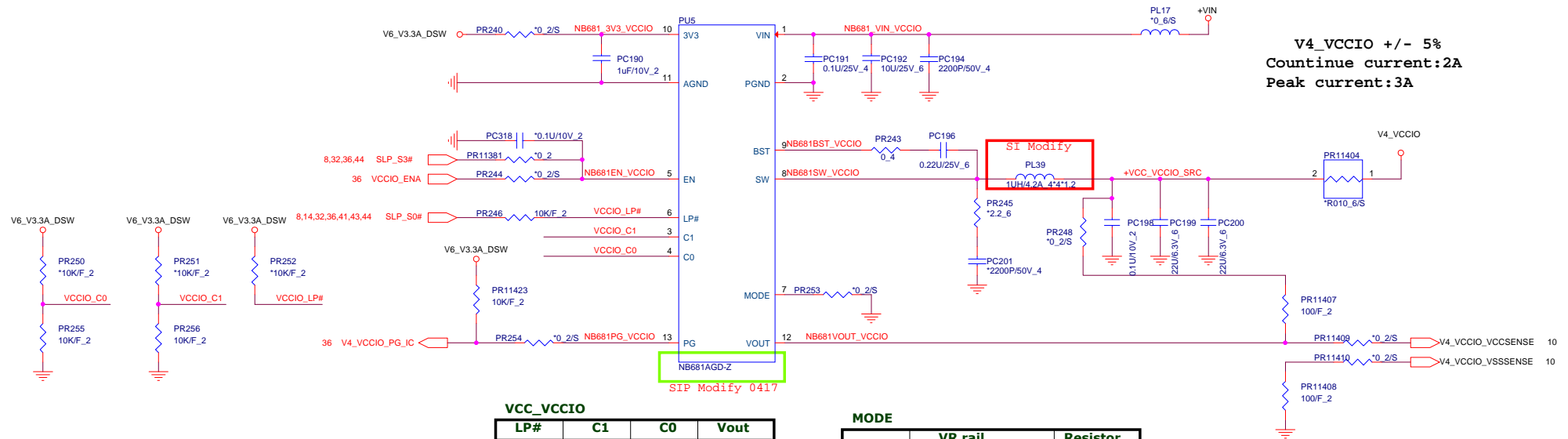
Net name	V(Typ.)	A(Typ.)
UFC_VDD_OUT	1.2V	0.15A
UFC_VIF_OUT	1.8V	0.05A
UFC_ANA_OUT	2.8V	A
WFC_VDD_OUT	1.2V	A
WFC_S_IO_OUT	1.8V	A
WFC_VCM_OUT	2.8V	0.5A
WFC_ANA_OUT	2.8V	0.2A

VCCSA



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	+VCCSA (NCP81253)	A
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VCC_VCCIO

LP#	C1	C0	Vout
0	X	X	0
1	0	0	0.85
1	0	1	0.875
1	1	0	0.95
1	1	1	0.975

MODE

	VR rail	Resistor
M1	VCCIO	0
M2	PRIMCORE	Float
M3	EDRAM/EOPPIO	100K
M4	other	150K

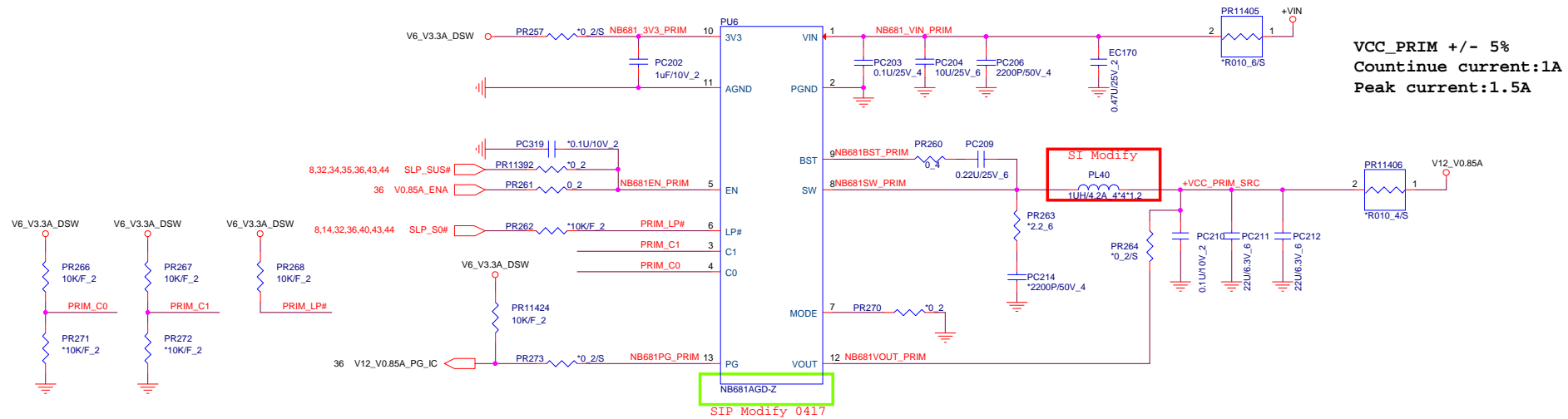
V4_VCCIO 2.7,10,32,36
 +VCC_VCCIO_SRC 10



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	+VCC_VCCIO (NB681)	A
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14,33,34,35,36,38,39,40,48 +VIN
4,32,33,34,36,44,48 LDO3V
10,41 V12_V0.85A



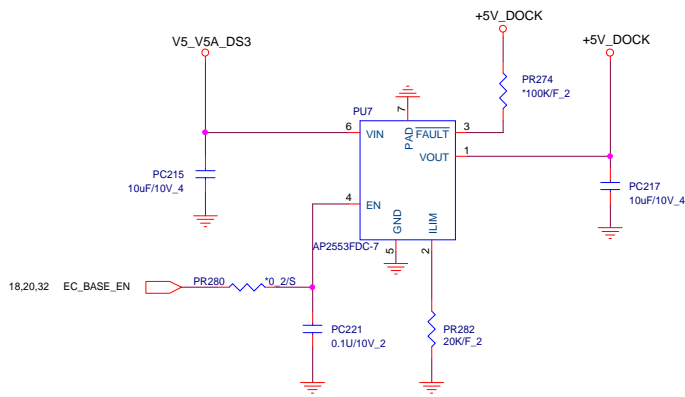
VccPRIM_CORE

LP#	C1	C0	Vout
0	X	X	0.7
1	0	0	0.85
1	0	1	0.9
1	1	0	0.95
1	1	1	1.00

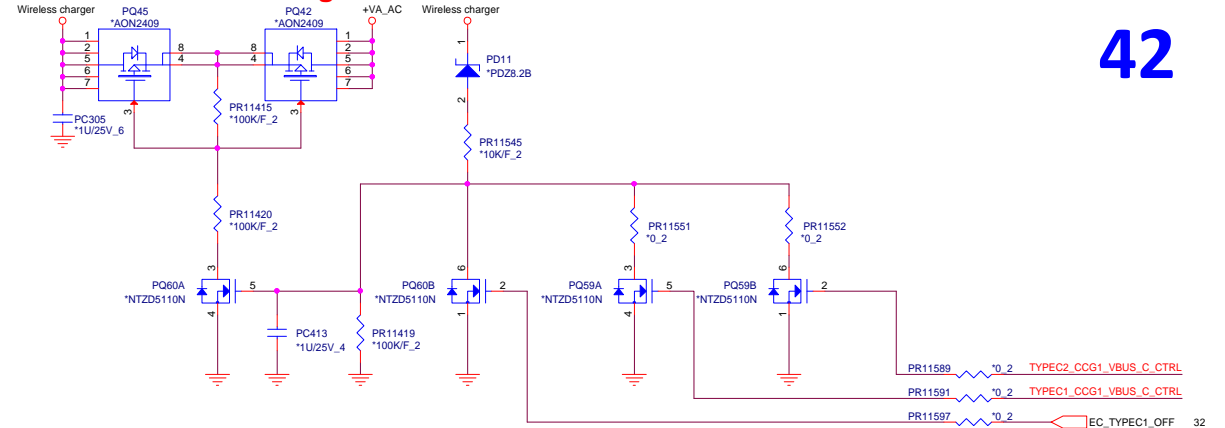
MODE

	VR rail	Resistor
M1	VCCIO	0
M2	PRIMCORE	Float
M3	EDRAM/EOPPIO	100K
M4	other	150K

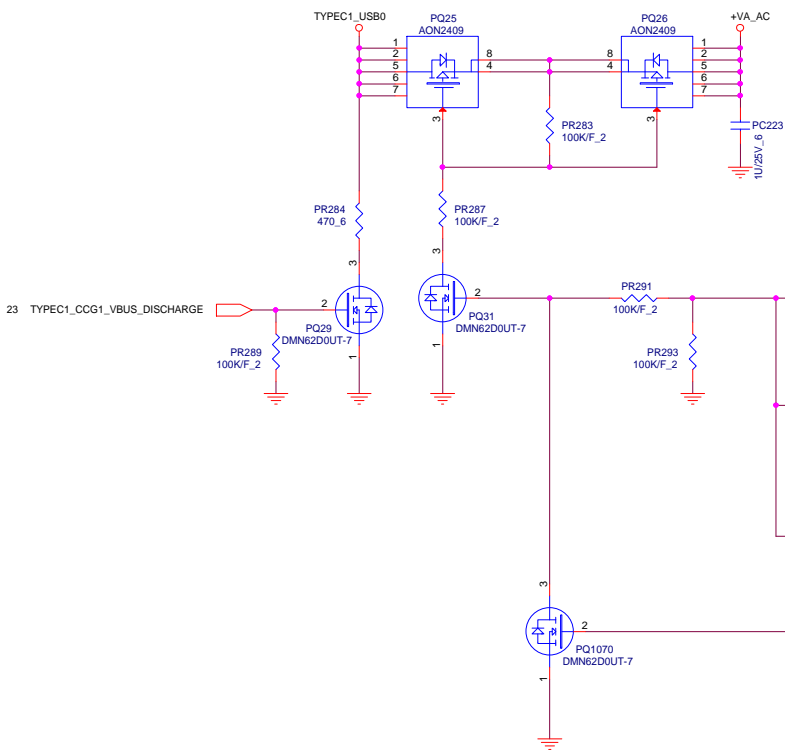
V12_V0.85A 10,41
+VCC_PRIM_SRC



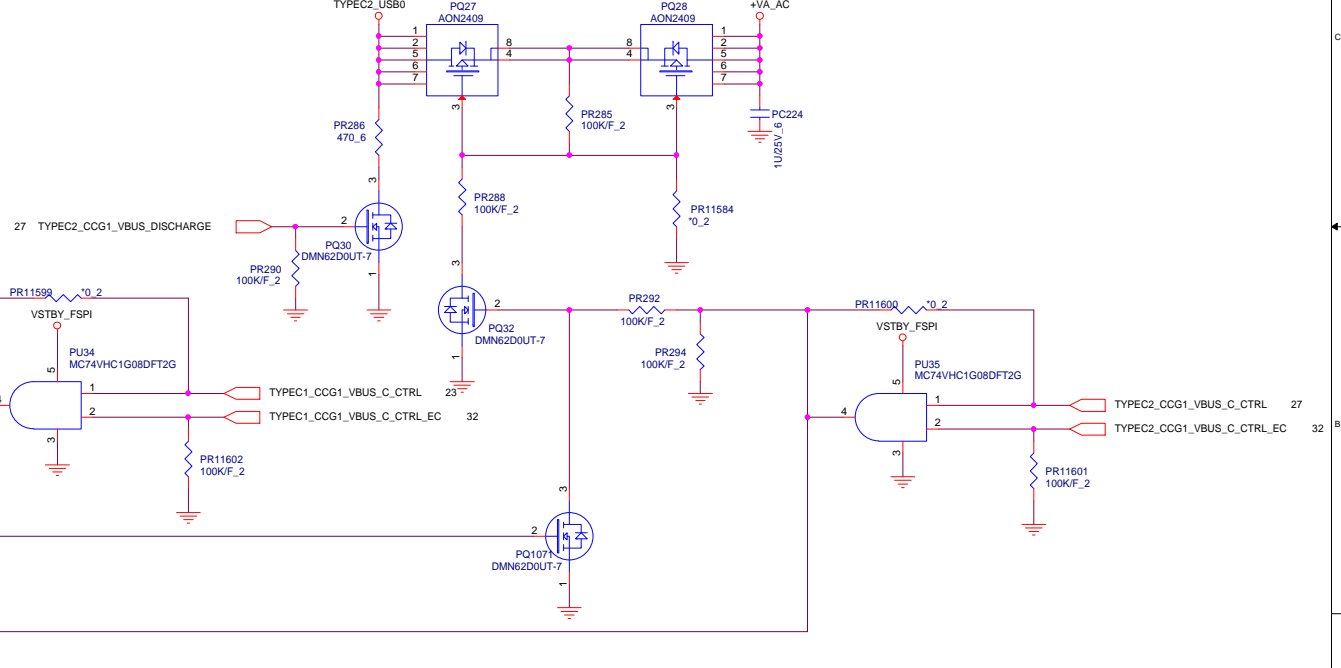
For Wireless Charger

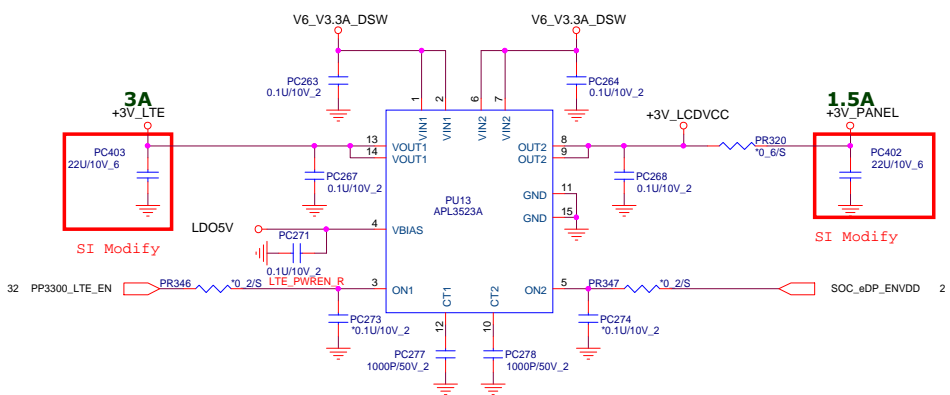
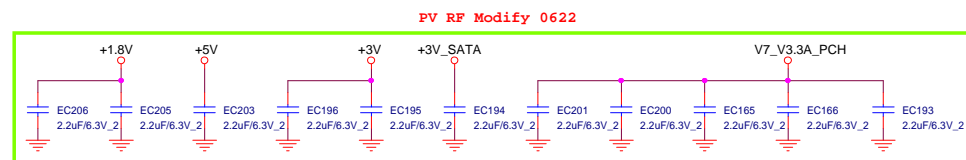
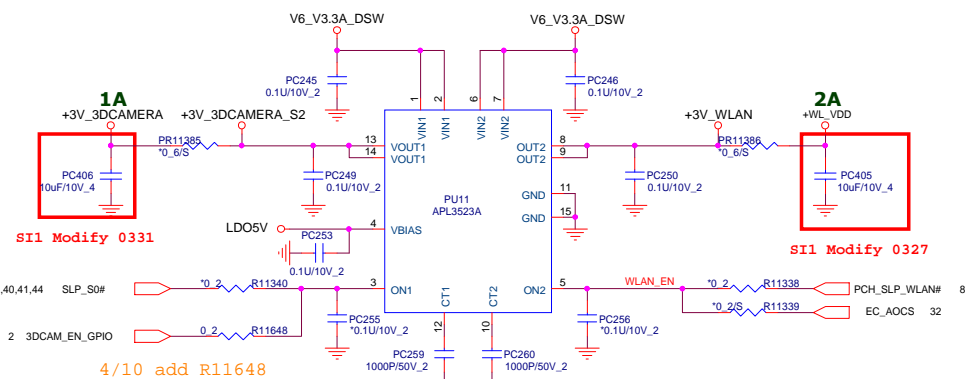
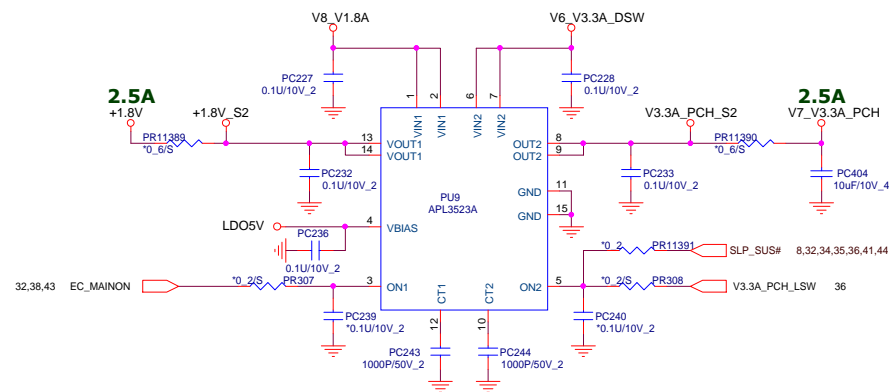
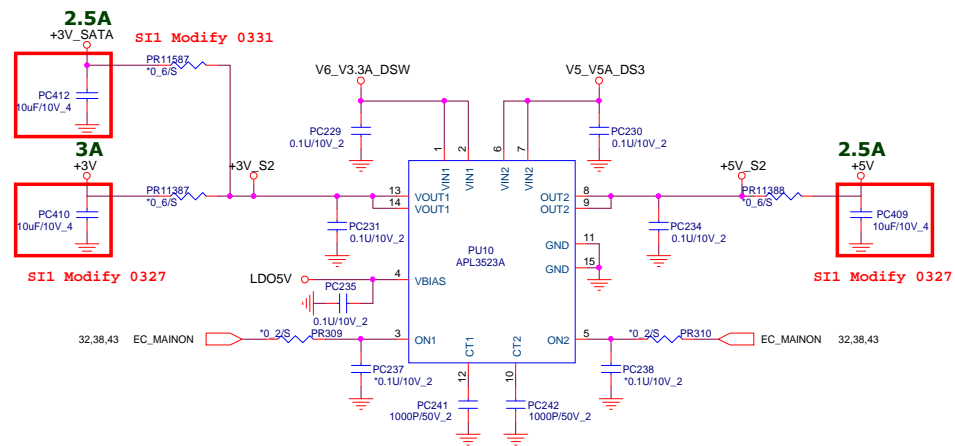


For TypeC PORT1



For TypeC PORT2





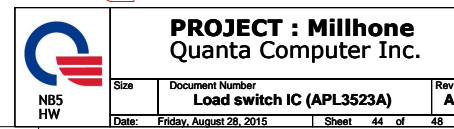
- +3V_3DCAMERA 16,37
- +3V_3DCAMERA_S2 17
- +3V_SATA 43
- +3V_S2 43
- +WLAN_VDD 18
- +3V_WLAN 14
- +3V_PANEL 14
- +3V_LCDVCC 14
- V7_V3.3A_PCH 2,4,5,6,8,10,14,18,19,23,24,27,28,36,37,44
- V3.3A_PCH_S2 2,4,5,6,7,8,11,14,15,19,20,22,31,32,36,37,38,43
- +3V 2,4,5,6,7,8,11,14,15,19,20,22,31,32,36,37,38,43
- +3V_S2 43
- +5V 20,43,45
- +5V_S2 20,43,45
- +1.8V 15,20,36
- +1.8V_S2 15,20,36

- 2,4,5,6,7,8,11,14,15,19,20,22,31,32,36,37,38,43 +3V
- 20,43,45 +3V
- 14,33,34,35,36,38,39,40,41,48 +VIN
- +3VS5
- +5VS5
- +3VLAVCC

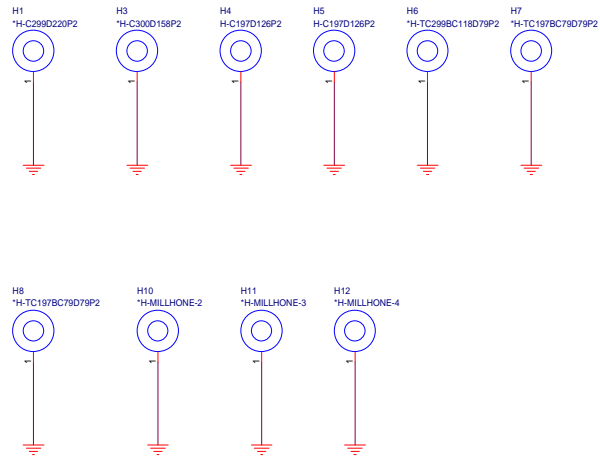


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Size	Document Number	Rev
	Load switch IC (APL3523A)	A
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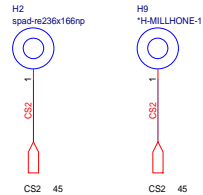


SCREW HOLE

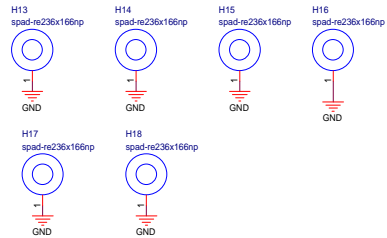


P-Sensor Spring

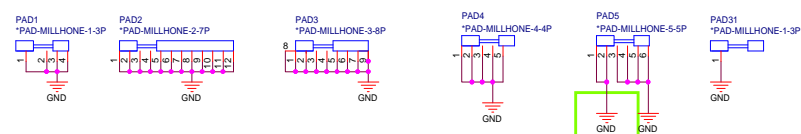
4/14 modify H2
footprint to spad-re236x166np



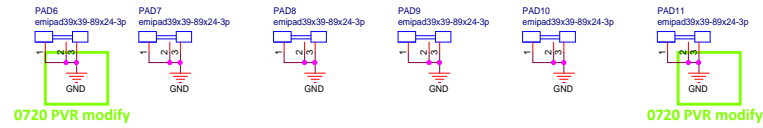
7/16 add gnd pad for RF



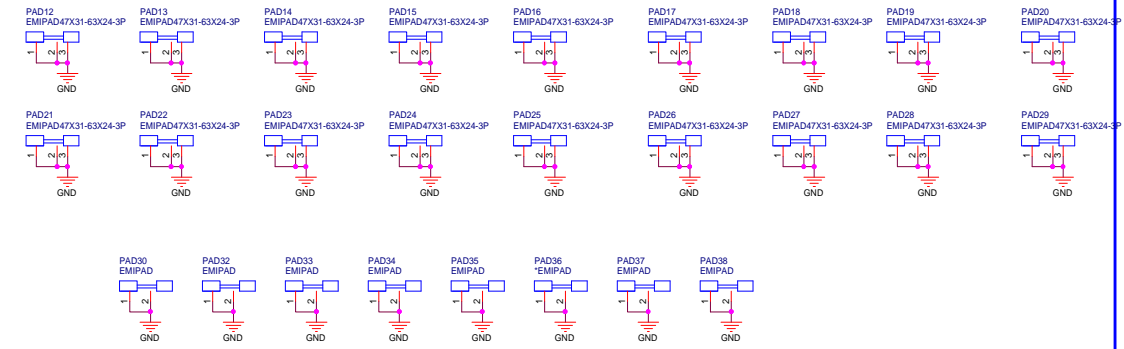
BOT SHIELDING PAD



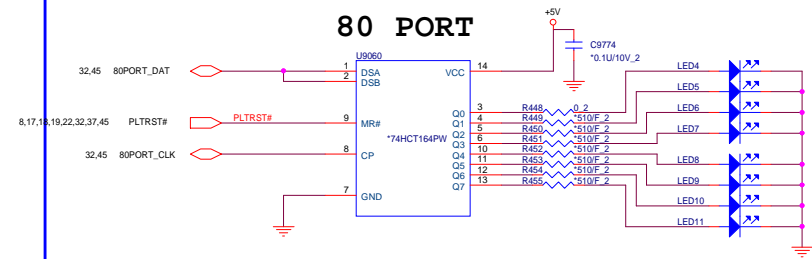
CLIP WLAN SHIELDING



CLIP THERMAL SHIELDING



80 PORT



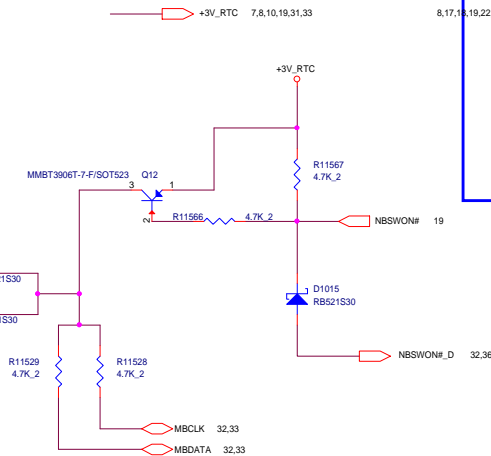
MV Modify_0817

Input	RD	CP	D	Output	Q
SD	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H

[1] H = HIGH voltage level;
L = LOW voltage level;
X = don't care.

Input	RD	CP	D	Output	Q _{n+1}	Q _{n+1}
SD	H	T	L	L	H	L
H	H	T	H	H	L	L

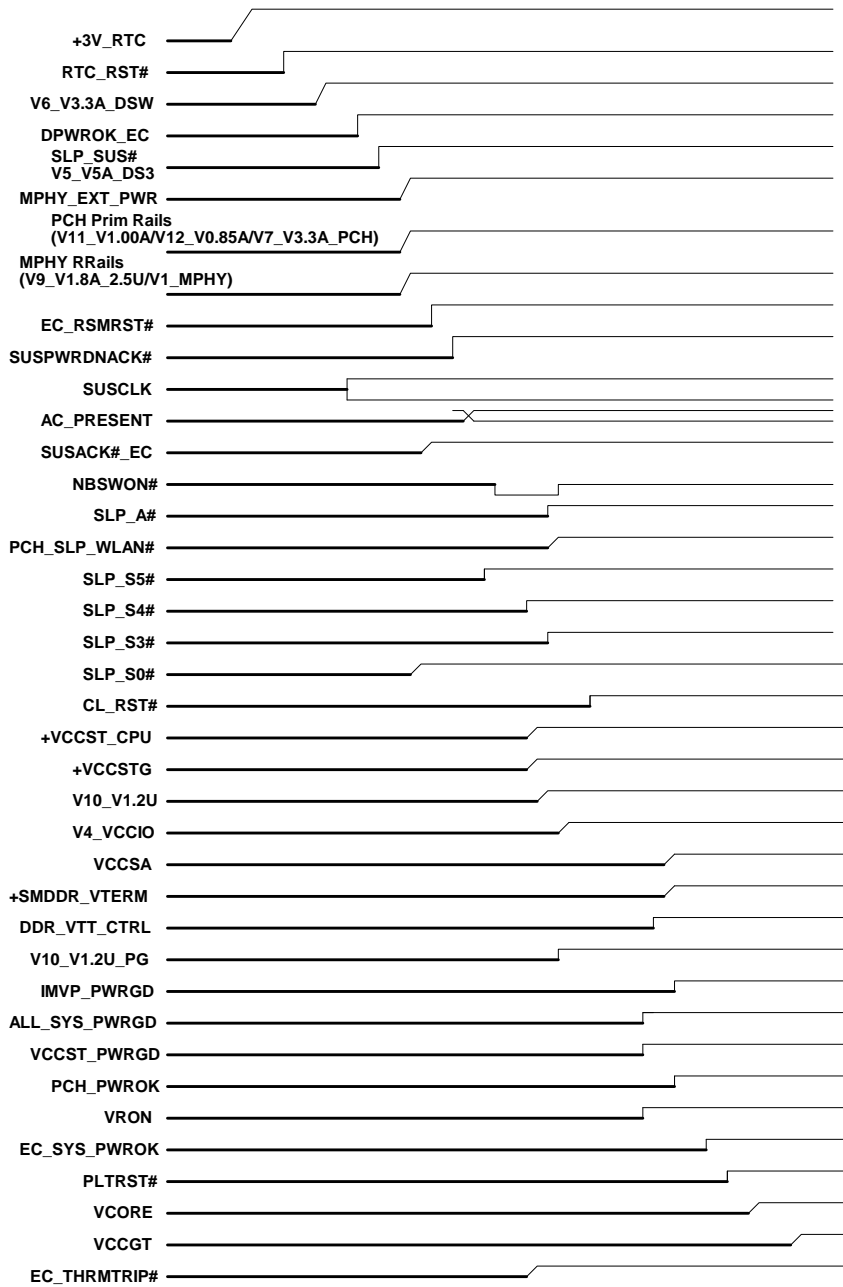
[1] H = HIGH voltage level;
L = LOW voltage level;
T = LOW-to-HIGH CP transition;
Q_{n+1} = state after the next LOW-to-HIGH CP transition.



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Millhone Power up sequence



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CPU Skylake-Y

